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Nanocrystalline silicon thin film transistors

by

Durga Prasanna Panda

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering

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Ames, Iowa

2006

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ABSTRACT

Flexible, large area circuits represent a new form of electronics which have led to rapidly rising and promising applications in displays, sensors, medical devices and other areas. The most important challenge in realizing these macroelectronic systems is fabricating the required thin film transistors on plastic substrates with a low thermal budget. Here most TFTs are fabricated using amorphous silicon (a-Si) as the active channel layer and amorphous silicon nitride as the gate dielectric layer. Low device mobility and electrical instability are the main disadvantages of a-Si TFT. Laser annealed polycrystalline silicon TFTs offer much better device performance and stability, and enable integration of driver circuits in the same process as the pixelated array. However, poly-Si suffers from poor uniformity across the substrate, lower/reduced device yield, and higher process complexity. Recently, direct-deposited nanocrystalline silicon (nc-Si) has been introduced as an attractive material alternative for the TFT active layer. While high electron mobility (~50cm^2/V-s) has been achieved in n-channel devices, the hole mobility in p-channel devices has been very low (~ 0.01cm^2/V-s) and thus unsuitable for CMOS applications.

In this thesis, we will describe the growth and properties of p-channel nc-Si thin film transistor (TFT) devices. In contrast to previous work, a significant improvement in the hole mobility was achieved by an innovative approach of depositing nc-Si for the channel material using very high hydrogen dilution and low ion bombardment in a PECVD reactor. The doping of the body was changed by doping with ppm levels of phosphorous, and the threshold voltage was found to change systematically as

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phosphorus content increased. We were thus able to show that a high-quality nanocrystalline silicon material can be controllably doped in small amounts. The TFT devices are of the bottom-gate type, grown on oxidized Si wafers. Source and drain contacts were provided by using either plasma grown p type nanocrystalline layers, or by the simple process of Al diffusion. A top layer of plasma-deposited silicon dioxide was found to decrease the off current significantly. High ON/OFF current ratios exceeding 10^6 were obtained. Hole mobilities in the devices were consistently good, with the best mobility being in the range of ~1.6 cm^2/V-s, which is the highest so far to the best of our knowledge.

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CHAPTER 1. INTRODUCTION

1.1 Research Motivation

Integrated backplane circuits are the key to the widespread application of large-area electronics, which presently comprises liquid crystal displays and X-ray detector arrays, but would eventually extend to sensor skin, electrotextiles and mechatronic materials. These large-area backplane circuits will be based on unit cells, or pixels, which contain the basic function and its control, with each cell containing some intelligence used for local signal processing in amplification, addressing and multiplexing [1]. In this scheme, a neighborhood of cells will be controlled by a higher performance circuit, and the entire backplane will be addressed by driver circuits. To make such backplanes available, pervasive circuit integration will be required [1]. A basic requirement of such integration is that a single transistor material and process be used for all hierarchical functions, ranging from driving circuitry to high speed switching and multiplexing. In other words, the backplane transistor technology should perform similarly to complementary metal-oxide-semiconductor (CMOS) circuits made in single-crystal silicon, and all this has to be done at sufficiently low temperatures compatible with inexpensive substrates.

Silicon, being the backbone of the semiconductor industry is a natural choice in achieving these objectives, and thus the need to go towards low temperature silicon processing. Over the years, amorphous, polycrystalline, and recently, nanocrystalline forms of silicon have gained prominence as low temperature alternatives to crystalline silicon for large-area applications. Amorphous silicon is the current material for most of

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the thin film transistors used in liquid crystal displays, and a host of other applications. It is a versatile material for limited mobility applications, and can be reliably grown at very low temperatures, but suffers from bias stress and light induced degradation. Polycrystalline silicon on the other hand has much higher mobilities, and hence suitable for high-speed CMOS applications. But it requires processing at much higher temperatures, which is out of scope of inexpensive plastic substrates. Although methods of converting amorphous silicon to polycrystalline silicon exist by laser induced crystallization, it suffers from problems of device uniformity besides being expensive.

For this reason we have been pursuing thin-film transistor technology based on nanocrystalline silicon, nc-Si:H as an inexpensive alternative. This semiconductor can provide sufficient electron mobility [1–3] and hole mobility to host CMOS circuits [2]. Moreover, it can be fabricated at low temperatures which are compatible with the plastic substrates envisaged for roll to-roll production [3]. However, nc-Si:H is a complex material whose deposition and device processing are not yet mature [4]. The high mobility material develops only after a certain film thickness with an associated problem of high transistor leakage current in the 'off' state [1]. With their top gate geometry, introduction of SiO_2 dielectric, and reduced tolerance to series resistances, high-mobility TFTs made from directly deposited nc-Si or from laser crystallized mc-Si pose much greater challenges to fabrication on plastic. Making the ancillary materials, including a stable gate dielectric and highly conducting contacts at temperatures of ~100°C may turn out to be more demanding on the fabrication of silicon TFT CMOS on plastic substrates than the preparation of the channel material itself [5].

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The next frontier of the flat panel display industry, flexible and conformal displays, extends the motivation for exploring CMOS and high-current capable Si TFTs to their fabrication at low temperatures using flexible foil substrates. Flexible displays are very attractive since flexibility is associated with light weight and ruggedness. These are desirable features for portable applications of today, and even more so for the large-area displays, e-textiles, and mechatronic materials of tomorrow.

1.2 TFT Structures

Unlike the conventional method of crystalline silicon Field-effect Transistor fabrication, many possible device geometries exist for TFTs using thin-film technology. These devices can be broadly classified into top-gate and bottom-gate types depending upon the placement of the gate dielectric relative to the channel material. In bottom-gate (inverted) devices, the gate dielectric is below the active layer, while in top-gate devices the gate dielectric layer is above the active layer similar to conventional MOSFETS. These can be further classified into coplanar and staggered types depending upon the location of the source and drain contacts relative to the gate. In coplanar TFTs, the source and drain contacts are on the same side of the active region as the gate contact, whereas in staggered structures, the source and drain contacts are on the opposite side of the active region as compared to the gate contact. These device geometries are schematically described in the following figure.

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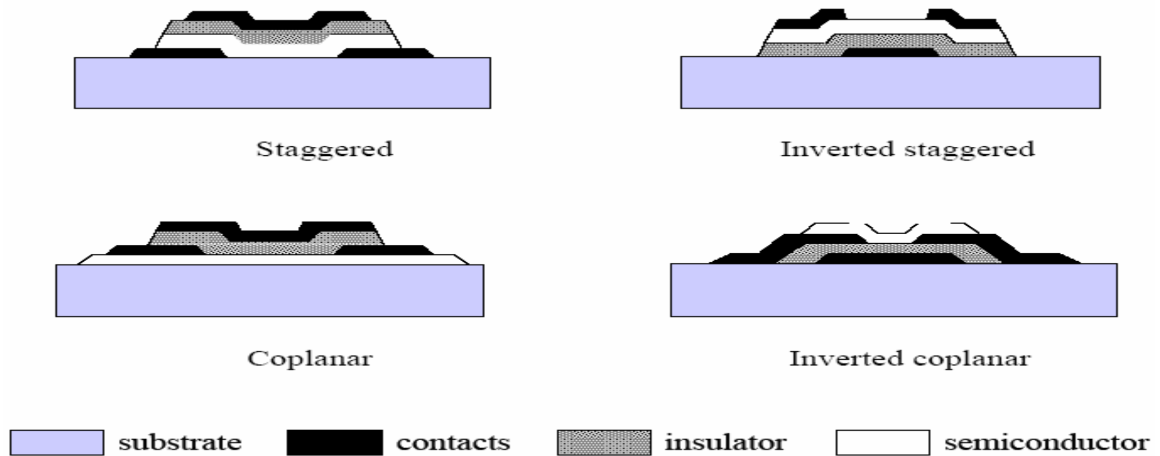

Figure 1 Schematic of commonly used TFT structures [6]

The inverted staggered structure is the most popular configuration for a-Si:H TFTs, and is currently the industry standard. One of the most important reasons for this is that silicon nitride forms an excellent gate dielectric with amorphous silicon which is currently the material of choice owing to low cost and low temperature fabrication. When silicon nitride is deposited by PECVD, the starting material is of very poor quality, and improves as it grows in thickness. If SiN_x is grown on top of an active layer, the channel formation interface layer will have many defects. This will lead to poor conduction and mobility in the channel, including increased susceptibility to gate bias stress effects. For this reason, the gate is first patterned on the substrate, followed by SiN_x dielectric and active layer deposition. This results in improved interface with good electron mobility (~1cm^2/V-s).

For nc-Si:H thin film transistors, silicon dioxide is the preferred gate dielectric on account of a better interface and higher stability. One of the above TFT structures is chosen, after a careful consideration of processing factors and materials involved. For top

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gate nc-Si:H TFTs, the most critical factor which dictates a particular design is the nc-Si:H and SiO_2 interface.

1.3 Literature Review

Although the concept dates back to 1935 [7], the study of thin film transistors (TFTs) blossomed in the late fifties, and early sixties [8,9] for potential replacement of the bipolar transistor. At that time, TFTs (based on thin films of III-V or II-VI compounds such as InAs, CdS or CdSe) were competing with single crystal Si MOS devices for logic circuit applications. The latter clearly emerged as the winner in the mid-sixties only. The principle of active matrix addressing was probably first put forward by Brody in 1969 [10].

In 1971, in a famous paper, Lechner and co-workers described and analysed the AMLCDs and proposed several possible approaches, including TFTs [11]. However, it is probably the first report, by LeComber and co-workers in 1979, of a a-Si:H TFT fabricated by plasma enhanced CVD at low temperature that triggered the development of the AMLCD industry. Since then, hundreds of millions of man-hours of research and development and a comparable amount of investment have brought the a-Si:H technology to a mature state.

Historically a-Si:H TFTs are used primarily as pixel switches, but researchers have explored them for current sources [12], on pixel amplifiers [13], and peripheral driver circuits [14,15]. The complementary circuits required for low-power operation are out of reach of a-Si:H because of its low electron mobility and its hole mobility is insufficient for any feasible p-channel device operation. Nanocrystalline (nc) and

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microcrystalline (mc) silicon, with their higher field-effect mobilities, considerably expand the range of application of silicon TFTs. nc- and mc-Si have been proved to be capable of p and n channel and thus of complementary metal insulator semiconductor (CMOS) operation. These devices when used for peripheral driver circuits can enable high-level on-glass integration. High-level integration has the dual benefit of raising yield and reducing cost. Additionaly, nc- and mc-Si TFTs are also capable of driving high-current loads such as organic light emitting diodes (OLEDs) for future displays. The following table summarizes the low-temperature silicon processes prevalent at present.

Table 1. Status of silicon materials for TFTs [5]:

Attribute	a-Si:H	nc-Si:H	μc-Si
Standard deposition T (°C)	250	250	150 (precursor)
Highest T process/material (°C)	350 SiN_x	280 n^+, p^+	Laser μc-Si
Lowest reported process T (°C)	110	150	Laser
Electron mobility ($cm^2 V^{-1} s^{-1}$)	0.5–1	40	300
Hole μ ($cm^2 V^{-1} s^{-1}$)	~0.01	0.2	50
Conductivity ($S cm^{-1}$)	10^{-11}	10^{-7}–10^{-2}	10^{-6}
Growth rate ($nm s^{-1}$)	0.1–1	0.1	0.1–1
Gate and source/drain geometry	Bottom Staggered	Top Coplanar or staggered	Top Coplanar
Gate insulator	SiN_x	SiO_2	SiO_2

Though a lot of research groups are engaged in research of nanocrystalline silicon thin film transistors, it is the group led by Sigurd Wagner at Princeton University who has done pioneering work in this field during the last seven years. They have demonstrated a maximum electron mobility of $40 cm^2V^{-1}s^{-1}$ for nc-Si top-gate TFTs [16], and for the first time, a reasonable hole mobility of $0.25 cm^2V^{-1}s^{-1}$ [16]. Another group led by Arokia

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Nathan at University of Waterloo, Canada have demonstrated for the first time a maximum electron mobility of $150cm^2V^{-1}s^{-1}$ in a very recent publication [17].

1.4 Scope of Research

The reported value for electron mobility at $40cm^2V^{-1}s^{-1}$ for top gate nanocrystalline silicon thin film transistors is quite reasonable and as verified by independent experiments. The highest reported value for hole mobility at $0.25cm^2V^{-1}s^{-1}$ is quite low and as the authors have acknowledged, this is due to poor contacts and low quality of silicon dioxide gate insulator deposited by RF PECVD. The highest value of hole mobility measured for nanocrystalline silicon using Time Resolved Microwave Conductance measurements is $2cm^2V^{-1}s^{-1}$.

A careful consideration of the above facts led us to the decision of focusing on p-channel nanocrystalline silicon thin film transistors and contributing to its improvement. Moreover, the fabrication itself revolves around involve a lot of materials with each of those having immense potential for improvement, as summarized below. Initially, we had devoted quite a lot of time in fabricating n-channel nanocrystalline silicon TFTs to make sure that the processing, at least was right. n-channel TFT on account of a higher mobility helped us troubleshoot as it would have been very difficult otherwise, for a p-channel TFT in view of its limited mobility.

1.4.1 Nanocrystalline Silicon

One of the biggest problems hindering nc-Si research is a lack of knowledge about the transport and conduction mechanism in this material. Some believe that conduction in nc-Si:H is primarily limited by the a-Si:H material, while others believe that the conduction is limited by the crystalline grains, or defects within the crystalline grains [5]. The conduction mechanism in nc-Si:H is very complex, and depends on many

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parameters including average grain size, crystalline fraction, degree of oxygen contamination, hydrogen concentration in film, defect density, crystallographic plane orientation, etc. Again, all of these are determined by the processing parameters such as RF plasma power, frequency, hydrogen dilution ratio, pressure, substrate temperature, etc. These are primarily processing and material science issues, and once resolved, one will be able to fully optimize the growth of nc-Si in order to have a material with predictable properties tailor-made for a particular application.

1.4.2 Highly Conducting nc-Si:H Contacts

To fully utilize the best channel layer performance from a TFT, it is very essential that the doped layers be highly conductive. Although current deposition techniques have matured to the extent so as to provide good quality nc-Si:H contacts at moderate temperatures (>250°C), low temperature performance(~100°C) in terms of conductivity is still a matter of concern. A lot of scope for improvement still remains, and in this work we would show how we increased the conductivity in nanocrystalline silicon doped p-layers by over two orders of magnitude at low deposition temperatures of 150°C.

1.4.3. Stable Gate Dielectric

All TFT technologies for plastic (silicon, organics, CdSe) share the need for a high quality gate dielectric made at ultra-low temperature. A promising direction is growing the silicon dioxide under hydrogen free conditions so as to improve the gate oxide breakdown characteristics. In this thesis, we would also describe some of our work in developing good quality silicon nitride and silicon dioxide dielectrics by RF PECVD. The gate dielectric will remain at the focus of TFT research for some time to come, regardless of the type of channel semiconductor.

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CHAPTER 2. MASK DESIGN AND TFT FABRICATION

2.1 Introduction

In order to obtain a high performance thin film transistor a proper design of the mask is absolutely critical. In addition to the proper material deposition steps, one has to ensure that the design margins are carefully maintained in the mask so as not to run into processing and lithographic issues like improper overlap, inadequate aspect ratios, among others. Before moving on to thin film transistor fabrication, masks were designed for both top-gate and bottom gate device configurations using L-Edit. Since the masks were printed from an outside vendor, four masking levels were incorporated in a single mask defined by chromium patterned on glass. The masks were designed to have channel lengths of 20µm, 30µm, 35µm 40µm and 45µm at a fixed channel width of 200µm. The devices were then distributed in random rows so as to check for processing uniformity and also to account for any characteristic location signatures that might arise. Here, would only describe the mask design for bottom-gate type thin film transistors and leave out the discussion for a similar mask designed for top gate type devices.

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2.2 Masking Levels and Dimensions

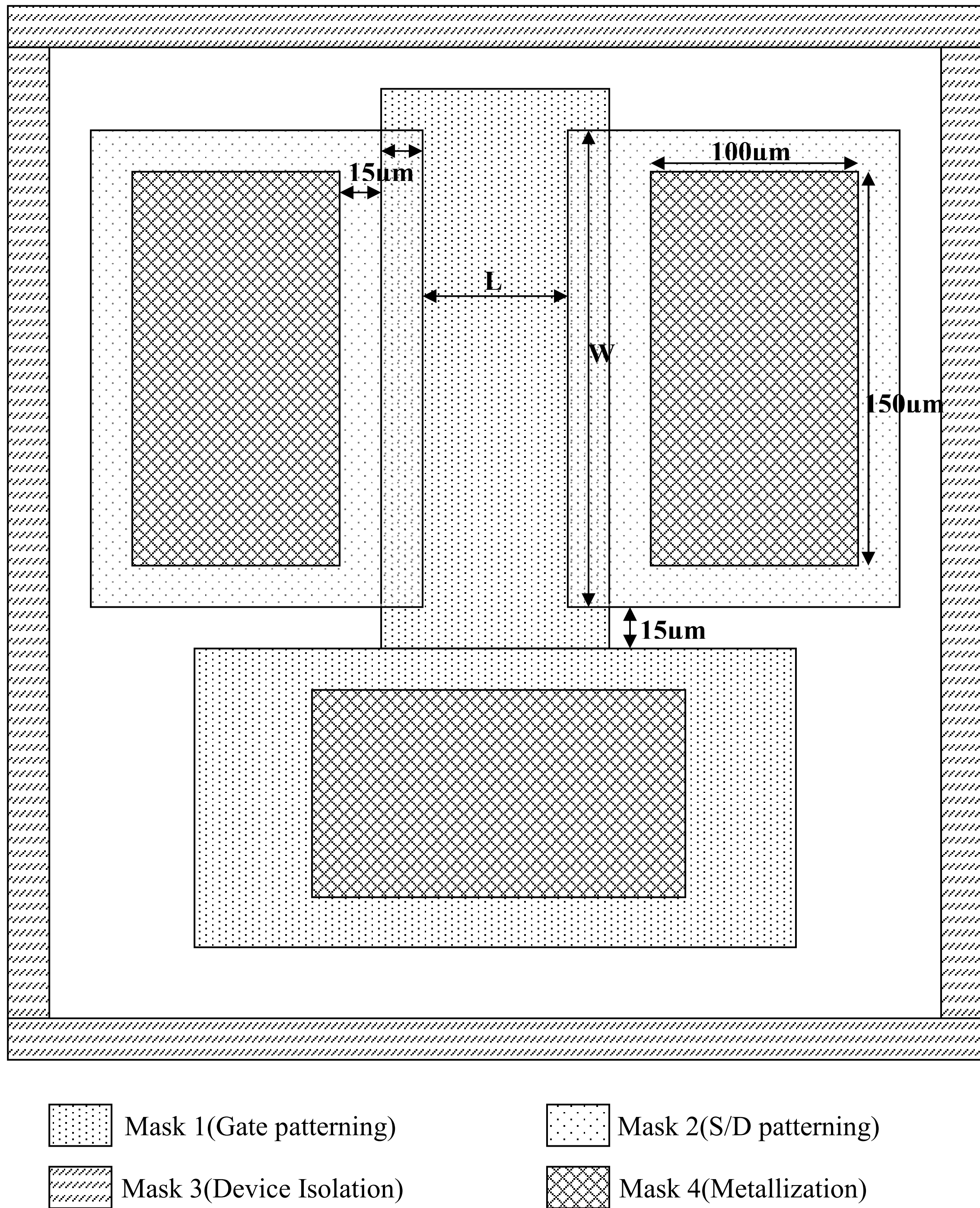

Figure 2.1 Schematic of masking layers and dimensions for bottom-gate TFT fabrication

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2.3 TFT Fabrication Overview

A brief description of the fabrication steps along with the detailed schematics involving the above masking layers is presented in the following:

1. Gate Oxide formation and nc-Si:H deposition: In this process, heavily doped p-type bare silicon wafers are cleaned by a standard RCA clean. The wafers are then loaded in a furnace and 1200Å of dry oxide is grown at a temperature of 1100°C. The wafers are then cooled down within the furnace in an ambient of nitrogen and hydrogen for 1 hour to improve oxide quality, and for the remaining time in nitrogen ambient, before gradually removing them at around 600°C. In the second step, the oxidized wafers are piranha cleaned followed by an ultrasonic in DI water before loading in the PECVD chamber. About 100nm of nc-Si is then deposited by a method described in a later section.

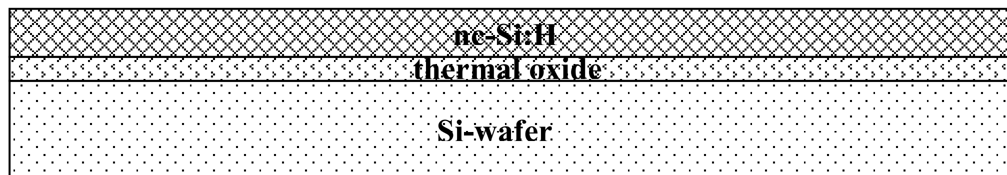

Figure 2.2 nc-Si:H deposited over thermally oxidized crystalline silicon wafer

2. Formation of active areas: In this step, we use the first mask to define the active regions using photolithography. The nc-Si:H is then selectively removed by using a wet etch recipe involving Hydrofluoric Acid, Nitric Acid, Acetic acid, and DI water. The purpose of this step is to isolate the devices, as would be discussed later.

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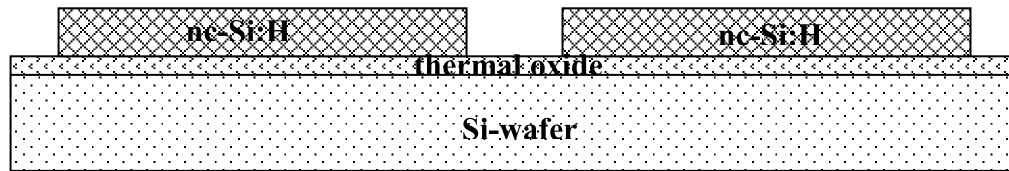

Figure 2.3 Active areas defined by photolithography and etching

3. Device Isolation and Passivation: After stripping the photoresist with acetone and methanol, a further piranha clean is performed followed by ultrasonic in DI water to remove contaminants. At this stage, the process was aborted if any peeling off was noticed in the nc-Si:H layer, because of doubts in its structural integrity. Then the wafers were loaded in the chamber to deposit around 3000Å of silicon-dioxide by RF-PECVD.

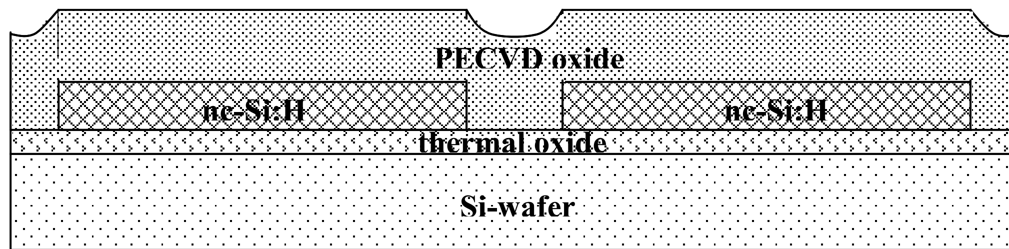

Figure 2.4 Device isolation and passivation by PECVD oxide

4. Source and Drain Patterning: At this stage the second masking level is introduced and regions for source and drain are opened up by photolithography followed by an Buffered Oxide Etch. The wafers are visually inspected for a complete removal of the oxide from exposed areas. The phororesist is then stripped followed by a Piranha clean, a slight BOE dip to remove any native oxide over the nc-Si:H surface and a DI water ultrasonic.

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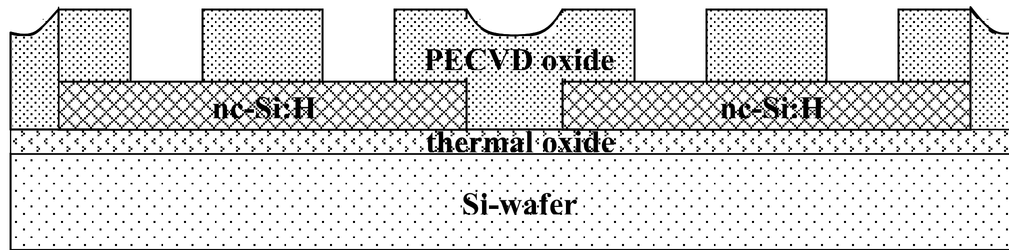

Figure 2.5 Opening of via in the oxide for source and drain regions

5. Contact formation: Now, the wafers are loaded in the deposition chamber and 75nm of heavily doped p-type nc-Si:H is deposited by ECR/VHF PECVD and would be described later. The wafers are then subjected to a BOE followed by a DI water rinse and loaded in the thermal evaporator. Now, 2100Å of Al or a mixture of 50Å of Cr and 2050Å of Al is sequentially evaporated, by a method described in a following section. It is worthwhile to note here that the gate metallization gets performed over the bare silicon wafer protected by a hard mask.

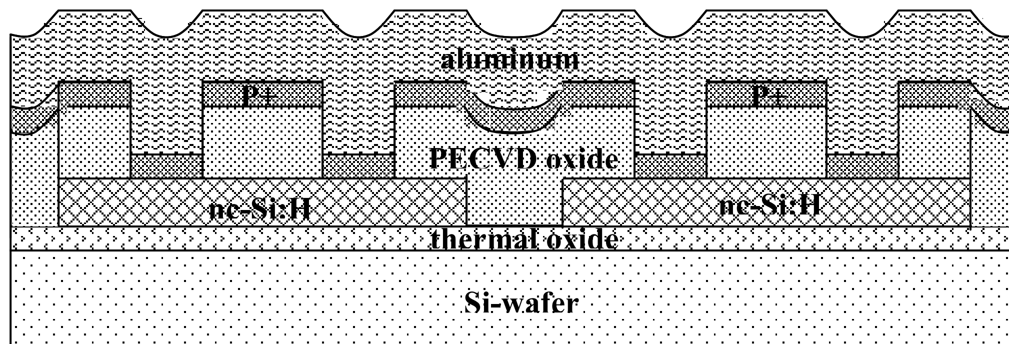

Figure 2.6 Doped material deposition and metallization

6. Final Device Formation: In this step, masking layer 3 is introduced, and the device is defined by photolithography. The selected areas are then subjected to an etch solution of Phosphoric, Acetic and Nitric acid (PAN etch) to expose the heavily doped p-type nc-

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Si:H layer underneath. A dry etch then follows to remove this nc-Si:H layer and isolate the devices. The devices are now ready to be probed after the photoresist strip.

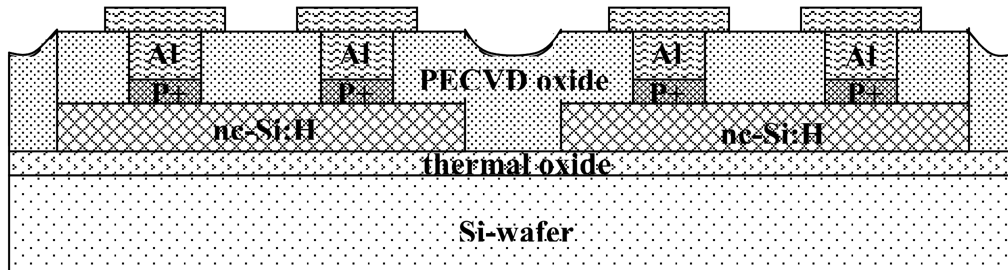

Figure 2.7 Cross section of the final device

2.4 TFT Processing

2.4.1 Plasma Enhanced Chemical Vapor Deposition

The goal of the plasma enhanced chemical vapor deposition was to deposit a film with desired properties on the surface of the wafer. In this work, chemical vapor deposition was used to deposit intrinsic and doped semiconductor films and dielectrics of silicon oxide and nitride. The chemical vapor deposition methods used were Very High Frequency PECVD, Radio Frequency PECVD and Electron Cyclotron Resonance PECVD. We would discuss these deposition techniques along with the process variables at length in the chapters to follow.

2.4.2 Metallization

The goal of the metallization step was twofold: firstly to deposit a thin conducting material onto the wafer for good contacts, and secondly to selectively dope the source and drain regions of the TFT as we would be discussing later. To serve as good contacts

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to the exterior world, the metal should deposit uniformly and conformally on the patterned surface. In addition to these, it should have a high conductivity, good adhesion to the bonding surface, and deposition should be free of voids and pinholes. In this work, we used aluminum and chromium for contacts to the TFTs. Aluminum, as we know diffuses into silicon upon annealing and dopes it p-type. Thus, for n-channel devices we used a sandwich structure of chromium and aluminum, where chromium served as the diffusion barrier to aluminum and also as contacts to heavily doped n-type nanocrystalline silicon source and drain regions. This prevented a diode type structure from forming at the interface upon anneal and kept the series resistances low.

We deposited aluminum and chromium in a thermal evaporation system. The operating base pressure for any metallization was carefully chosen to be 1×10^{-6} Torr. The low chamber pressure is important because of several reasons. One of these is the mean free path of metal molecules would be longer at a lower pressure enabling uniform deposition. More importantly, a low base pressure ensures that most of the oxygen molecules have been gettered out of the chamber; otherwise metal-oxides would result, and particularly, aluminum oxide is a very good insulator. In addition to this, an important step is the degassing of chromium rods. Chromium has the ability to attract moisture, and when heated releases water vapor into the chamber causing contamination to any evaporation performed during this time. For good quality contacts, and devoid of pinholes, aluminum was evaporated at 15-20Å/sec, and chromium between 3-5Å/sec.

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2.4.3 Photolithography

The goal of the most important photolighography process was twofold. First, to create on the wafer surface a pattern, whose dimensions are as close to the design requirements as possible and second, to align the pattern on the wafer to the correct spot. Photolithography was performed in the NSF lab with a Karl Suss mask aligner with standard operating procedures, the details of which have can be found from the appropriate manual. The critical parameters in our work was a 20 minute prebake at 90^oC and a 25 minute postbake at 120^oC after exposure and develop.

An important next step is a check on the quality of pattern transfer after postbake and before doing any subsequent etching steps. The patterned wafers are inspected under an optical microscope to identify problems associated with the photolithography stage. At that point if any abnormalities were found on the wafer due to the resist, the wafer could be "reworked", which means that the existing resist can be stripped off with acetone and methanol followed by DI water rinse, and the same lithographic process can be performed on the wafer again. During this visual inspection any problems such as misalignment, residues, pattern dimension deviations, poorly defined patterns, and scratches are all grounds for rejecting the wafer and redoing the process.

2.4.4 Wet etching

The goal of the wet etch was to selectively and permanently transfer the pattern of the mask onto the exposed surfaces of the wafer. For an ideal pattern transfer we expect an etchant to cut the sidewalls vertically and replicate the original dimensions on the mask. Wet-etch by its chemical nature cuts through all exposed areas equally and is isotropic. Dry etch, as would be discussed later can be tuned to anisotropic by varying various process parameters. We used wet etch for most of our work since it is

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inexpensive, less time consuming, and for most cases a slight lateral undercut compared to the device dimensions does not matter much. Both the metal layers in the transistor, chromium and aluminum were etched by a wet-process. Nanocrystalline silicon was also wet etched occasionally, depending upon the feasibility of the process.

The wet etching chemistry involves transport of reactants to the surface where the reaction takes place, and transport of the reaction by-products from the reaction zone. The key ingredients in any wet etchant is an oxidizer (HNO_3, H_2O_2), acid or base to dissolve oxidized surface (HCl, NH_4OH) and a dilutent media through products can be transported (H_2O, CH_3COOH). Most etching reactions are electrochemical, involving transfer of electrons during surface reactions. It can either proceed with oxidation involving a gain in electrons or through reduction involving a loss of electrons or by both in a redox reaction.

For performing a wet etch we immersed the wafer in a freshly prepared wet etchant solution with the appropriate type and amount of constituents. For the chrome etch, CEP-200 chrome etchant (manufactured by Microchrome Technology Inc.) was used. The aluminum etchant was prepared by mixing phosphoric acid, acetic acid, nitric acid and water in a solution of 4:4:1:1. This wet etchant for aluminum is commonly referred to as a PAN etch. Although, we had calibrated the etch rate of different materials, a visual inspection was used to determined the end point of a particular etch. To enhance etching uniformity, the immersion tank was agitated slightly during the duration of etch.

Wet etch is isotropic and therefore some amount of undercutting takes place depending upon the etch rate and the time for which the wafer is immersed in the etchant. The exactness of the image transfer is thus dependent on factors such as over-etching, under-etching, lateral undercutting, and/or isotropic etching of the sidewalls. Since a

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certain amount of undercutting is inevitable, a careful consideration of this was taken into account during mask design to avoid any device failures and appropriate margins were maintained in the dimensions of the transistor. Excessive undercutting will occur if the resist bond to the wafer surface fails, in which case the resist lifts off. This form of undercutting can be catastrophic to the transistor, and the so the remaining steps were aborted if this problem was found after an optical inspection following etch.

Incomplete etching is a very serious condition for the transistor, since it would result in a short or an open circuit depending upon the material being etched. Therefore, we performed a slight amount of over-etch to discount the possibility of having an under-etch. Causes of an incomplete etch may include too short an etch time, presence of a surface layer that slows the etching, thickness variations, and/or a weak etch solution. Severe over-etching can take place when the etch time is too long, or the etch solution is too strong.

2.4.5 Dry etching

The goal of dry etching is the same as wet etching, i.e. to permanently transfer the pattern of the mask to the surface layer of the wafer. However, the means by which this is accomplished differs from wet etching. Unlike wet etching, reactive ion etching can be a combination of chemical etching coupled with plasma energy for sputtering and hence etching by ion bombardment. Therefore, in reactive ion based etching, we have a chemical or isotropic component and a sputtering or anisotropic component. A delicate balance has to be achieved between the two for etching a given material with required selectivity and etch profile.

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We used a reactive ion etch (RIE) system for dry etching nanocrystalline silicon and silicon nitride in our process of fabricating thin film transistors. Depending on the material to be etched a different set of etch parameters including gas chemistry, power (ion density), and pressure were used. All of these parameters along with the design of the RIE system will determine the etch rate of a material. Before dry etching could begin on the device wafer the etch rates of the nc-Si:H and (n^+/p^+) nc-Si:H needed to be determined. The same samples that were used to determine the growth rate were also used in determining the etch rate. The samples were loaded into the RIE system and were etched for ten minute duration, following which, a thickness measurement was performed. The samples were again etched for a five minute duration, and the etch rate determined in each case after measuring the thickness by optical means. Table 2.1 shows the etch parameters and etch rates for the materials used in the transistor.

Table 2.1: RIE Parameters and Etch Rates

Film (Etch Rate)	Pressure	RF Power	DC Voltage	Gas Flow
nc-Si:H (218 Å/min)	25 mTorr	35 Watts	125 Volts	O_2 (4sccm) CF_4 (50sccm)
(n+) a-Si:H (246 Å/min)	25 mTorr	35 Watts	125 Volts	O_2 (4sccm) CF_4 (50sccm)
(p+) nc-Si:H (225 Å/min)	25 mTorr	35 Watts	125 Volts	O_2 (4sccm) CF_4 (50sccm)
Silicon Nitride (>433 Å/min)	25 mTorr	50 Watts	100 Volts	O_2 (7.5sccm) CF_4 (50sccm) NF_3 (5sccm)

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CHAPTER 3. CHEMICAL VAPOR DEPOSITION

3.1 Introduction

Chemical Vapor Deposition is defined as the formation of a solid film on a substrate by the reaction of vapor-phase chemicals (reactants) that contain the required constituents [19]. In a typical CVD process the reactant gases introduced into a reactant chamber are decomposed and/or reacted at a heated surface to form the thin film. During this process, the reactants do not react with the substrate material in bulk and hence no substrate material is consumed.

The fundamental principles of chemical vapor deposition involve a lot of physics and chemistry including thermodynamics, heat transfer, gas-phase reactions, surface and plasma reactions, nucleation and growth, among others. Each process has to be carefully understood and optimized to deposit a film with given/expected properties. We would briefly touch upon the basic aspects of CVD for a better appreciation of growth and film properties discussed in later chapters.

Before proceeding it is worthwhile to mention the relative advantages of CVD over other thin film deposition methods such as sputtering, evaporation, growth from a liquid phase, etc. In spite of some practical problems such as complexity and expensive, CVD is the method of choice because of a better conformality [20, 21] and the ability to deposit in holes and trenches. This is unlike other physical vapor deposition approaches which are highly directional. Moreover, CVD introduces beneficial impurities, unlike for example sputtering, where silicon films are defective in an atomic scale with poor electronic properties due to broken or dangling bonds. CVD films of silicon have

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additions of hydrogen which terminate these dangling bonds, resulting in good quality films. There are however many examples where a particular deposition method is chosen depending upon the requirements in hand.

In this work we have deposited nanocrystalline silicon using Very High Frequency (VHF) CVD, silicon dioxide and silicon nitride using Radio-Frequency (RF) CVD, and doped layers using Electron-Cyclotron-Resonance PECVD. The principle behind these plasma deposition schemes would be outlined briefly in this chapter, along with the advantages of using a particular technique over another.

3.2 Fundamental Aspects of CVD

In a typical CVD reactor, the film formation proceeds sequentially through the following steps and as illustrated below:

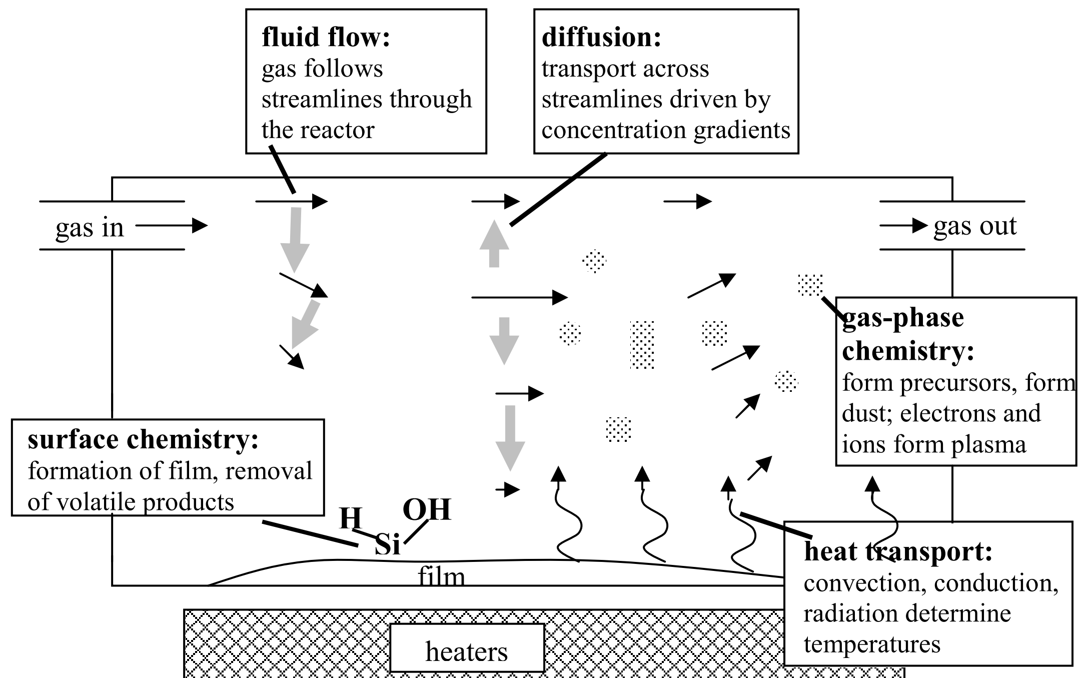

Figure 3.1 Processes occurring in a typical CVD reactor [20]

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Firstly a given set of gases are introduced through the inlet which flows by forced convection to the outlet [19].These reactant gases reach the surface of the substrate by gas-phase diffusion through the boundary layer and are adsorbed on the substrate surface as adatoms. By surface migration, these adatoms reach the growth sites where the film-forming chemical reactions are taking place resulting in solid film and gaseous byproducts. The gaseous byproducts are desorbed from the surface, diffuse through the boundary layer region near the surface and are removed with gas flow at the outlet.

Energy for driving the film formation reactions can be supplied by thermal energy, photons or electrons or a combination of these. In this context, it is important to note that reactions can also occur in gas phase (homogenous reactions) in addition to those near the surface of the substrate (heterogenous reaction). Homogenous reactions produce dust which can get incorporated in the growing film leading to defects, poor adhesion and should be avoided. In addition, homogenous reactions can cause unwanted reduction in deposition rate due to consumption of reactants, whereas heterogeneous reactions are highly selective. Our aim therefore, was to minimize gas phase reactions by a judicious adjustment of deposition parameters.

3.2.1 Thin film nucleation

A closer look into the film formation mechanism suggests that the adatoms continue to move along the surface either due to kinetic energy from their lateral velocity or due to thermal activation from the surface. These adatoms while in motion can interact with other adatoms and form stable clusters, which are called nuclei, by a mechanism known as nucleation. The Gibbs theory of nucleation suggests that for molecular clusters

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larger than a critical size, the total energy of the system decreases with increasing size, energetically favoring growth. If the critical radius is not reached, atom clusters are more likely to shrink and re-evaporate.

The film growth stage begins after the formation of critical sized nuclei. This is accompanied by the island stage where nuclei grow in three dimensions, but growth parallel to the substrate exceeds that normal to the surface. In the island step, the nuclei can have well defined crystallographic shapes, and is a result of diffusion of adatoms along the surface. The next stage is coalescence, where nuclei join each other and form larger shapes. The area projected on the surface is reduced, and an increase in height of the deposit occurs. The reduction in surface area uncovers fresh substrate for nucleation sites resulting in formation of a continuous film, by a process known as secondary nucleation.

3.2.2 Structure of thin films

Thin films in general, have smaller grain size as compared to bulk. Grain size is a function of the deposition temperature and also post-deposition anneal, increasing with temperature as a result of increased surface mobility. The grain sizes also increase with thickness of the film and saturates after a certain thickness, indicating that new grains nucleate upon existing ones. The growth rate also plays an important role in determining grain size. At higher deposition rates, the clusters are quickly buried under subsequent layers even if they might have sufficient mobility.

The surface roughness of a film arises due to the randomness of the deposition process. Although this represents a higher energy state than a perfectly flat film, real films always have surface roughness associated with them. High temperature deposition

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leads to lower surface roughness because the increased surface mobility helps in filling the peaks and valleys. Films deposited at low temperatures show an increase in surface roughness with thickness.

The crystallographic structure of thin films depends on the mobility of atoms and can vary from a highly disordered or amorphous structure to a well-ordered state. This well-ordered or crystalline state can also exhibit grain orientations in preferential directions depending upon the growth variables. Deposited dielectrics such as SiO_2 and Si_3N_4 have an amorphous structure, while most metal thin films are polycrystalline. Silicon can have either an amorphous, polycrystalline, or single crystal structure depending on the deposition parameters and substrate material.

3.3 Plasma Fundamentals

The word "plasma" was first applied to ionized gas by Dr. Irving Langmuir, an American chemist and physicist, in 1929. Plasma consists of a collection of free-moving electrons and ions, i.e. atoms that have lost electrons. Energy is needed to strip electrons from atoms to make plasma. The energy can be of various origins: thermal, electrical, or light (ultraviolet light or intense visible light from a laser). With insufficient sustaining power, plasmas recombine into neutral gas.

Plasmas can be broadly divided into “thermal” and “cold” varieties. A thermal plasma is so hot that the average thermal energy of electrons (kT) is high enough to separate electrons from their atoms on a regular basis. In cold plasmas, only the electrons are hot, with neutrals and ions being at temperatures much lower than their ionization energies. This happens as the electrons on account of a much lighter mass are very inefficient in transferring energy to the much heavier species. Moreover, if the ratio of the

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system size to the mean free path is small enough, the electrons don't have enough time to transfer energy to the ions before recombining at the walls or being pumped away. This discrepancy between electron and gas temperatures make cold plasmas of great interest for planar processing, particularly for chemical vapor deposition. Hot electrons can ionize, dissociate and excite, including a lot of interesting chemistry that doesn't take place otherwise in a cool gas. In practical systems, these plasmas occur at pressures well below atmosphere, and the reactor types are classified according to the mechanism by which they couple energy into the electrons.

3.3.1 Capacitively excited plasma reactor

The most widely used plasma reactor for CVD applications is the capacitive or "RF diode" plasma reactor. In this system, the plasma is generated by applying an AC or RF voltage between two electrodes in a parallel plate configuration, as shown in the following figure. The frequency of the signal can range from a few Hz to many MHz, and the two electrodes can either be of the same size or of different sizes.

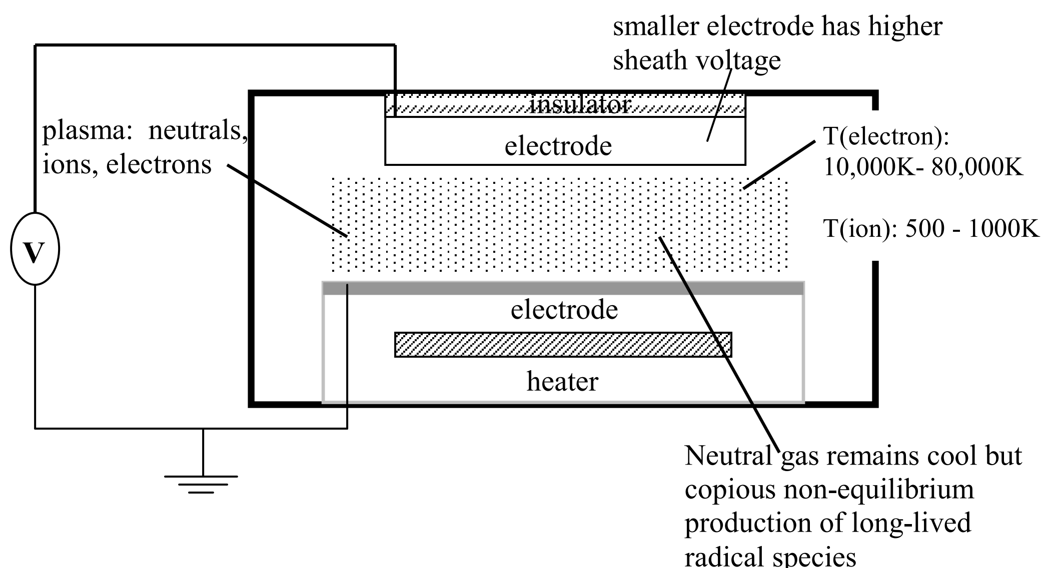

Figure 3.2 Simplified view of a generic capacitively-excited plasma [20]

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The plasma forms "sheaths", which are regions of very low electron density, next to solid surfaces. The RF voltage mostly appears between these sheaths in a way similar to the dielectric region of a capacitor, with the electrode and the plasma forming the two plates as shown in figure 3.2.

The ions roll down-hill in the sheath regions and acquire energy in this process which is dissipated at the walls. The electrons float upwards and are confined by the potential away from the sheath regions, which therefore have few electrons. The plasma is therefore the most positive object in the system, with the sheath potential varying during the RF cycle.

For CVD applications, the system pressure is usually between 20mTorr and 10Torr. The gap between the electrodes is an important parameter and varies from 0.5cm to 10cm, usually getting smaller for high pressure operation. Typical gaps are a few hundred times the mean free path and so it is the product of the chamber pressure and the electrode distance which is important in designing a system.

Typical electron temperatures are around 5eV, and the ion density is equal to the electron density in the plasma to maintain overall charge neutrality. Though most atoms and molecules have ionization energies ranging from 5eV to 20eV, around 100eV of energy is required to produce an ion and a new electron, due to energy loss and inefficient energy transfer. The density of electrons and ions is known as the plasma density. The plasma density depends upon a fine balance between the input power which heats up electrons and provides energy to ionize, and the loss of ions to the walls. In typical capacitive plasmas, the plasma density is very low, with about 0.01% fractional

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ionization. Fractional excitation can be much higher, since excitation and dissociation require much less energy than ionization.

3.3.2 Effect of excitation frequency

The actual potential across the sheath vary with time and add up to the applied RF voltage. Since the plasma is always more positive than any of the electrodes, one sheath grows and the other shrinks as we go through the RF cycle. For ac excitation at tens of KHz, the ions and electrons have time to leak out and the plasma density varies with the AC cycle. For frequencies >>100KHz, there is not enough time for electrons and ions to be lost in different parts of the sinusoidal cycle, and many RF cycles are required by the ions to cross the sheath. So, the kinetic energy in this case reflects the time average potential unlike the instantaneous potential exhibited at low frequencies. This explains the fact that higher frequencies lead to lower ion energy, and less bombardment at the substrate.

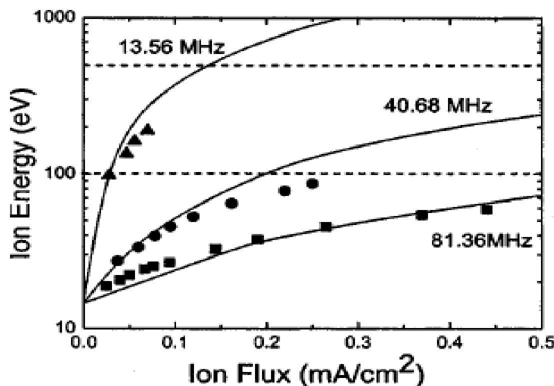

Figure 3.3 Ion energy as a function of ion flux and excitation frequency [22]

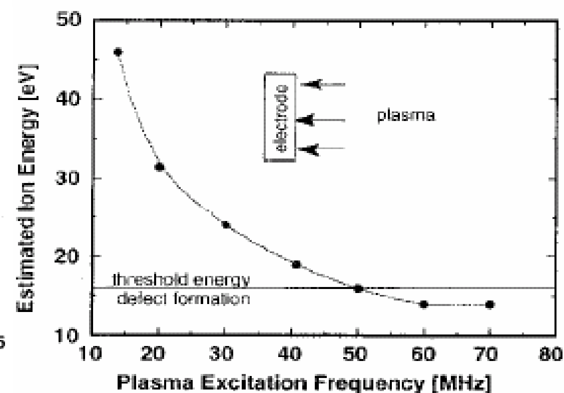

Figure 3.4 Ion energy as a function of plasma excitation frequency [22]

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Also, as frequency increases into the MHz range, two new mechanisms for transferring energy to the electron assume significance. Firstly, the change in sheath size during each RF cycle results in a displacement current flow as the charges move back and forth through the plasma. This displacement current can be quite significant [19] ($3mA/cm^2$), and much larger than the sheath ion currents. This displacement current can cause heat dissipation as it encounters resistance in the plasma. Since the power is proportional to square of the current, and the current is proportional to the frequency, the power dissipated scales as the square of the frequency.

Secondly, the sheath velocities at high frequencies approach electron thermal velocities (10^7cm/sec). As a result, electrons in the plasma can scatter from the sheath and gain energy. In the same way the electrons can also give up energy to the sheath when it is moving away, but the number of electrons being encountered by the sheath is higher when it moves into the plasma instead of moving out. Sheath reflection is localized near the moving sheath edge and also scales as the square of the frequency.

3.3.3 Influence of deposition pressure:

In this section we would discuss the very important effect that chamber pressure has on the growth of nanocrystalline silicon thin films deposited by PECVD. For this part of the work, we deposited nc-Si:H in a parallel plate VHF-PECVD reactor using a mixture of silane and hydrogen at a temperature of 300°C. Thermally oxidized crystalline silicon wafers were used as substrates, and the plasma power was kept fixed at 22W. The films were grown with silane to hydrogen dilution ratio of 99% using a VHF frequency of 45.9MHz. The deposition was done at pressures of 100mTorr and 300mTorr

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respectively and the films were compared using Raman Spectroscopy and X-Ray Diffraction.

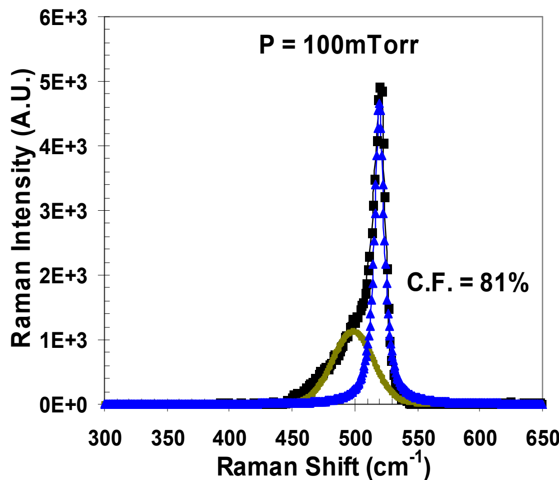

Figure 3.5 Raman Spectra of nc-Si:H film deposited at 100mTorr

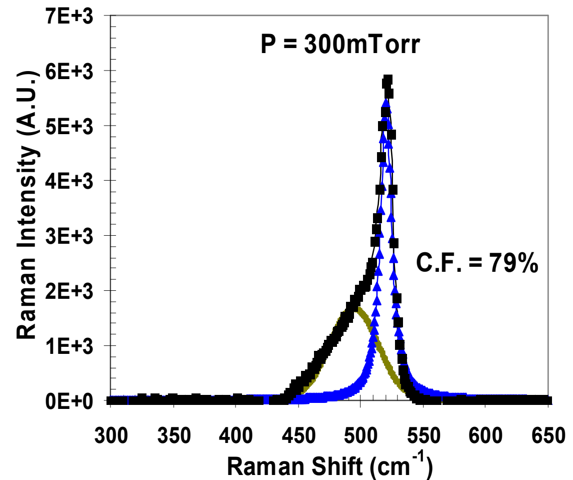

Figure 3.6 Raman Spectra of nc-Si:H film deposited at 300mTorr

The Raman spectra for both the films are shown in figure 3.5 and figure 3.6 with the prominent crystalline peak at ~520cm^{-1} accompanied by an amorphous phase at ~480cm^{-1}. A comparison of crystalline fraction from the Raman spectra of the two films reveals that both of the films had achieved approximately the same degree of crystallinity. It may be mentioned here that upon increasing the pressure to more than 300mTorr, the crystalline fraction decreases for depositions done under the same power conditions. This happens because the ion bombardment level falls below the critical level to achieve best crystalline films. We have thus found out that the power has to be increased slightly with increase in pressure to maintain the critical level of ion bombardment required to promote predominantly nanocrystalline phase formation.

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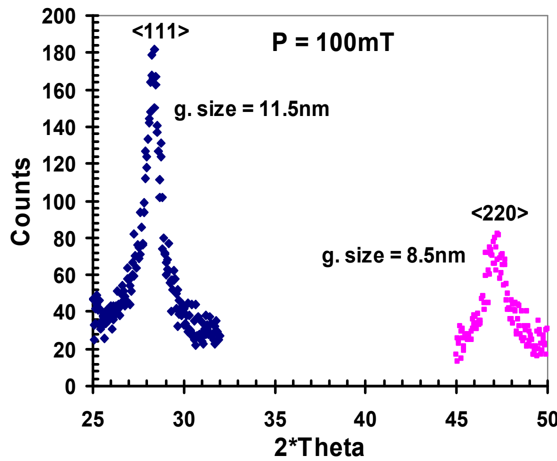

Figure 3.7 XRD of nc-Si:H film grown at a pressure of 100mTorr

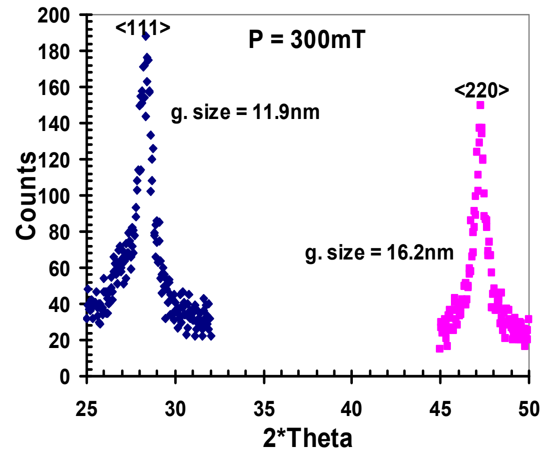

Figure 3.8 XRD of nc-Si:H film grown at a pressure of 300mTorr

Figure 3.7, and figure 3.8 show the results of X-Ray diffraction performed on the two films grown at high and low pressures under otherwise identical conditions. For the film grown at a pressure of 100mTorr, the grains were predominantly oriented in the <111> direction with a small fraction of the grains being oriented in the <220> direction with grain sizes of 11.5nm and 8.5nm respectively. Now, as the deposition pressure is increased to 300mTorr, we have a couple of interesting observations: the grains are still oriented in the <111> and <220> directions, although the <220> grains start becoming more prominent. Most importantly, the <220> grain size have now doubled as compared to the previous case, and are now 16.2nm. The <110> grain sizes of 11.9nm are comparable to the low pressure deposition at 100mTorr.

Therefore at high pressures, we find a tendency of the grains to orient towards the <220> direction which is thermodynamically more stable accompanied by an increase in size. This can be explained by the fact that at higher pressures, the films have more chance to relax and thus attain thermodynamically preferred orientations. The electron

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mobility is expected to be higher along the <220> direction as compared to <111>, and also increase with grain size. An interesting experiment in the future could be in depositing nc-Si:H channel layers for TFT at increasing pressures and then correlating the mobility to the grain size and orientation to gain more fundamental insights into the material and transport mechanisms.

3.4 Electron Cyclotron Resonance (ECR) CVD

3.4.1 Operation principle

The ECR source operates on microwave energy coupled to the natural resonant frequency of the plasma electrons in presence of a static magnetic field. As shown in the following figure, a charged particle moving with a constant velocity (v), perpendicular to a uniform magnetic field (B) experiences a Lorentz force. The electron with mass m_e, would orbit in a circular path with Larmour radius, r_c given by $r_c = mev/qB$, and with an angular frequency $w_o = qB/me$. Typical values of the Larmour frequency are 280 MHz at a magnetic field of 100 Gauss or 2.8 GHz at 1000 Gauss [20]. Under the condition that the pressure is sufficiently low for electrons to complete their orbits without scattering, the electromagnetic field at Larmour frequency is in phase with the electron motion and adds energy on each orbit. ECR reactors typically operate at a microwave frequency of 2.47 GHz.

The application of magnetic fields to the plasma results in “trapping” of the electrons. They are thus forced to circle around the field lines instead of diffusing freely to the walls. The ions are less influenced by the magnetic field since they have much larger Larmour orbits and shorter mean free paths. Therefore, the probability that a

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molecule can be ionized by a hot electron increases due to the increased path length, and so the plasma can be sustained at very low pressures (few mTorr) where conventional capacitive plasmas are difficult to ignite. Shown below is the simplified diagram for our ECR-PECVD reactor.

3.4.2 Experimental setup

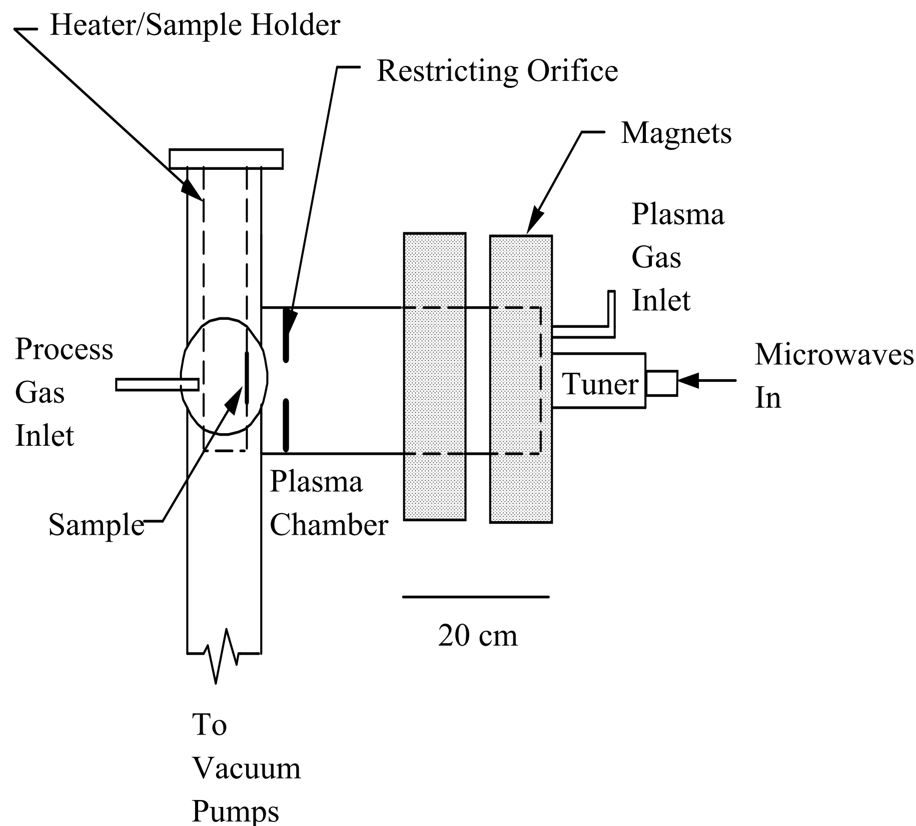

Figure 3.7 Simplified diagram of the ECR-PECVD reactor used in this work

3.4.3 Discussion

Though capacitive plasma reactors are simple to build and are versatile, they suffer from some significant limitations. Especially at low pressures, increasing the RF power does not necessarily increase the plasma density with the power getting wasted in

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enhanced ion bombardment and hot electron creation instead of contributing to ionization. The plasma potential can become very high and lead to contamination of substrates by sputtering of chamber walls. The ECR method of creating discharges can help us to circumvent many of these limitations, some of which are [23]: 1. Higher ion density of over an order of magnitude more as compared to rf-plasma because of the fact that electrons can absorb more efficiently from the microwave source from resonance. 2. Low ion energy (10-50eV) leads to growth of films, especially oxides with good microstructure and other mechanical properties. 3. The operational gas pressure in ECR reactors is a few mTorr, which helps prevent unwanted gas phase reactions. 4. A high degree of gas decomposition approaching 100% can be achieved which improves the gas utilization and film growth rate. 5. Ion density and ion energy can be independently controlled and 6.Lower contamination due to the absence of electrodes. In this work, we have deposited heavily doped p-type nanocrystalline silicon films using ECR-PECVD and the processing details would be covered in a later chapter.

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CHAPTER 4. DIELECTRIC CHARACTERIZATION

4.1 Introduction

The gate-dielectric is the most important component of a thin-film transistor and governs the electrical characteristics of the device. Without a good gate-dielectric, transistor performance would be irreproducible and very unpredictable. Before proceeding with fabrication of the TFT a lot of research was done on the gate dielectric material that was to be used in the transistor. Primarily, the gate dielectric had to satisfy two important requirements among a host of others. Firstly, the gate material has to form a good interface with silicon with minimal density of surface states, so as to have a low threshold voltage. Secondly, it must have high breakdown strength for stability and keep the leakage current at low levels. In order to arrive at a best quality gate dielectric material, two important characteristics were primarily investigated:

1. The quality of the gate-dielectric interface with silicon
2. The gate-dielectric breakdown strength

In order to test a dielectric for these two properties, it was incorporated into both a metal insulator metal (MIM) structure and a metal insulator semiconductor (MIS) structure, and two tests were performed: fast interface state density test, and dielectric breakdown test. The results presented here are for the best samples of silicon dioxide and silicon nitride. The method of arriving at the optimum parameters is rigorously described in the following two chapters. After growing and testing several different dielectrics by

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RF-CVD, a decision was made as to which dielectric possessed the best qualities based on these two criteria.

4.2 Dielectric Breakdown Test

Significant electron tunneling can take place when a large electric field is applied across an oxide layer, eventually reaching a point of catastrophic dielectric breakdown. Once the dielectric breaks down, large conduction currents can pass through it rendering the device useless, and in irreversible. Therefore a high electric breakdown is a desired and useful property. It should be noted that the breakdown strength is not an average characteristic over the device area, but is governed by the weakest defect spot across its surface [24]. The field across the dielectric at which the breakdown occurs is the breakdown field.

We generally observe two types of dielectric breakdown characteristics in silicon devices [25]. In the first type, the dielectric breaks down rather abruptly, either on the current-time plot or on the current-voltage plot. In the second type, the dielectric breaks down gradually or softly and can be observed with similar plots mentioned above. Generally thick oxides (>100nm) break down abruptly, but thin oxides (10nm) often show soft breakdown behavior. In soft breakdown characteristics, the current keeps on increasing until the measurement is limited by the compliance limit of the current meter. For this reason, a dielectric can be defined to have broken down once the current through it has exceeded some arbitrary, but conveniently measurable unit. Usually, this value is defined at 10^{-10}A/cm^2 [26] of current through the dielectric by most authors, and we

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would go by the same definition in our work unless there is any abrupt breakdown observed.

In this test the breakdown strength of PECVD silicon dioxide and silicon nitride was examined by ramping up the gate voltage on a MIM structure until breakdown occurred or we had reached the limit of maximum voltage. An HP 4156A parameter analyzer was used to ramp up the gate voltage and measure the gate current.

The electric field breakdown of the silicon nitride ranged from 3.8 MV/cm to 5.2 MV/cm for the devices tested, and over 4.5MV/cm for the silicon dioxide samples. For dielectrics with low defects the breakdown field can be as high as 10 MV/cm or more [24]. Dielectrics with pinholes typically have breakdown fields around 1 MV/cm [24].

An important parameter to note is the ramp rate of the applied voltage when evaluating the dielectric breakdown. A smaller ramp rate results in reduced breakdown strength, as it corresponds to a longer stressing time and hence more charge injection until breakdown [24]. For our experiments on dielectric breakdown a ramp rate of 100mV/s was used.

4.3 Interface State Density Test

At the Si-SiO_2 interface, the lattice of bulk silicon and all the properties associated with its periodicity terminate [21], and localized states with energy in the forbidden energy gap are introduced at or very near to the interface. Thus, interface defect density refers to the number of atoms with dangling or unsatisfied bonds per unit area at the interface of two materials. The charge of the defect or trap can be positive, negative, or neutral, and might even change during device operation [21]. Dielectrics having an

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excellent interface with silicon have defect densities in the order of 10^9-10^{10} $cm^{-2}eV^{-1}$ [21].

There are several reasons why reducing the interface defect density is important:

• Traps can terminate electric field lines from the gate or contribute to them resulting in an altered threshold voltage [28].

• The trapped electrons and holes in these surface states can act as charged scattering centers for the mobile carriers in the surface channel and thus lower their mobility [29].

• The interface states can act as localized generation-recombination centers, thereby adding a surface leakage current to the device [30].

In view of the above, it is very important to minimize interface state defect density by an appropriate fabrication process in order to have predictable and reproducible transistor behavior. In general for a given fabrication process, the interface trap density depends to a great extent on the orientation of the substrate orientation. The interface state defect density is the lowest for crystalline silicon oriented in the <100> plane, followed by <110>, and being the highest in <111> oriented planes [25]. In this work, our PECVD deposited nanocrystalline silicon was predominantly oriented in the <220> and <111> directions, and is therefore expected to have a higher interface defect density as compared to <100> oriented crystalline silicon. Hydrogen atoms are very effective at tying up loose or dangling bonds at the dielectric/semiconductor interface, and can play a role in reducing the interface defect density [25, 27].

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4.4 Estimation of Interface State Defect Density

In order to characterize the interface between the semiconductor and insulator a capacitance-voltage or CV method was used. In this method two sets of CV curves were measured: one with a low frequency AC signal superimposed on the DC gate voltage (quasistatic) and the other with a high frequency AC signal superimposed on the DC gate voltage. Due to difference in carrier response times, different CV curves resulted from the low and high frequency cases. An approximate interface defect density value was then calculated from the difference in the two curves.

We used a MIS capacitor structure for our C-V measurements, where I stands for an insulator and is either silicon dioxide or silicon nitride. A band diagram of a p-type metal oxide semiconductor (MOS) capacitor with interface states under a positive gate bias is shown in figure 4.1 [31].

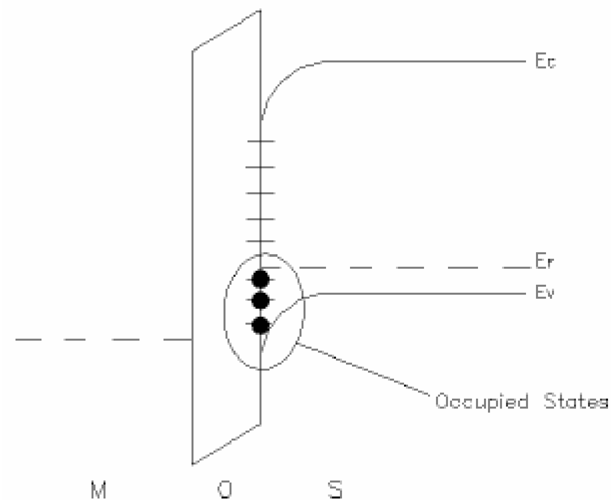

Figure 4.1 Band diagram of a p-type MOS capacitor [31]

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As the surface potential is varied, the fast interface states or traps in the band gap can move above or below E_F in response to the gate bias, since their positions relative to the band edges are fixed (figure 4.1) [31]. According to Fermi-Dirac statistics Energy levels above E_F tend to be empty or in other words, fast interface states moving above E_F tend to give up its trapped electron, while fast interface states moving below E_F tend to capture an electron. Interface trap charges are states that have a trapped electron or hole. Since charge storage results in capacitance, the fast interface states give rise to an additional capacitance in the MIS structure. This additional capacitance is in parallel with the depletion capacitance in the channel [31], with the combination being in series with the insulator capacitance, C_i. The equivalent circuit diagram for the three capacitances (C_i = insulator, C_{it} = interface traps, C_d = depletion) associated with the MIS capacitor is shown schematically in figure 4.2 [31].

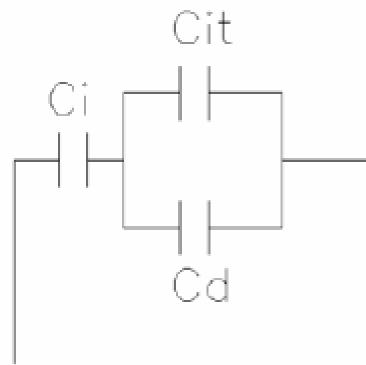

Figure 4.2 Equivalent circuit diagram of MOS capacitor [31]

It should be noted that the interface defects which are able to change their charge state relatively fast in response to changes in the gate bias are termed fast interface states. These fast interface states can keep pace with low frequency variations of the gate bias

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(1-1000 Hz), but not at extremely high frequencies (~1 MHz). Only those interface traps that can be filled and emptied at a rate faster than the capacitance-measurement signal can contribute to C_{it}, therefore the interface states only contribute to the low frequency case [31]. Inversion is only reached at low frequencies since the minority carriers needed for the inversion process are generated in the bulk of the semiconductor and if the frequency is too fast the minority carriers will recombine before participating in the inversion process. An important observation in this context is that we can notice inversion even at high frequencies in a MOSFET by grounding the source and drain electrode and performing C-V measurements on the gate electrode. This is because of the fact that the source and drain can supply the required minority carriers for inversion.

Since the interface defect density affects the CV curves of both the low and high frequency cases differently, the interface defect density (D_{IT}) can be determined from the difference in the two curves. An approximate value for the defect density is given by the following equation [31]:

$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{LF}}{C_i - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right) cm^{-2} eV^{-1}$$

Here, C_{HF} and C_{LF} are the capacitance values of the high and low frequency curves at the threshold voltage and C_i is the capacitance value of the MIS capacitor under strong accumulation. Figure 4.3(b) illustrates typical low and high frequency curves for a p-type MIS capacitor [31].

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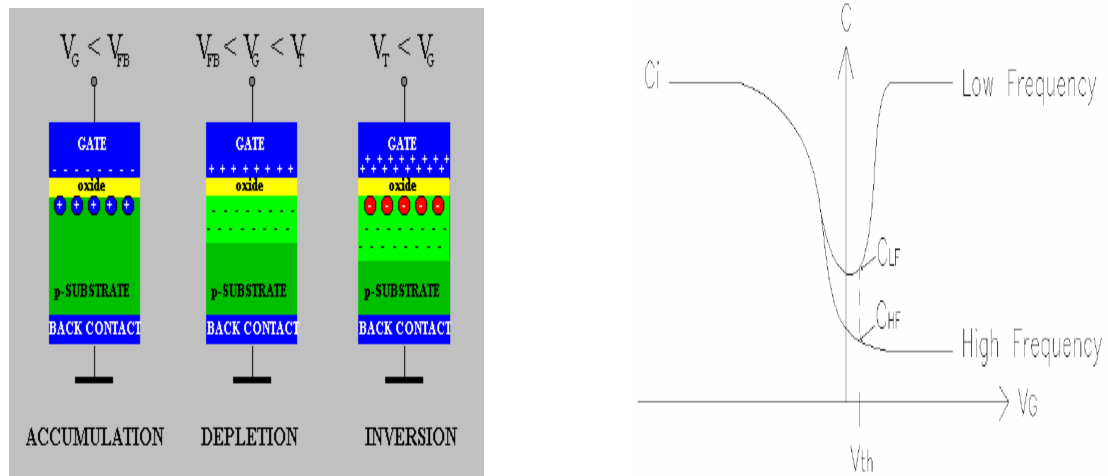

Figure 4.3 (a) MOS operation [32] (b) Typical high and low frequency curves for a p-MOS capacitor [8]

4.5 PECVD Oxide Defect Density

The following figure shows the experimentally observed C-V characteristics for our PECVD oxide with best overall properties. The MOS capacitor was fabricated on p-type crystalline silicon wafers with silicon dioxide deposited by RF-PECVD at a frequency of 13.6MHz, and a power density of 50mW/cm^2. The SiH_4/N_2O ratio was 30 and the ratio of He/SiH_4 was 200 with a deposition pressure of 400mTorr. Al was used for the top gate electrode and, chromium used as the bottom electrode was evaporated on the back-side of the wafer doped heavily by boron diffusion. A more detailed discussion on the deposition parameters would follow in the chapter on PECVD oxides.

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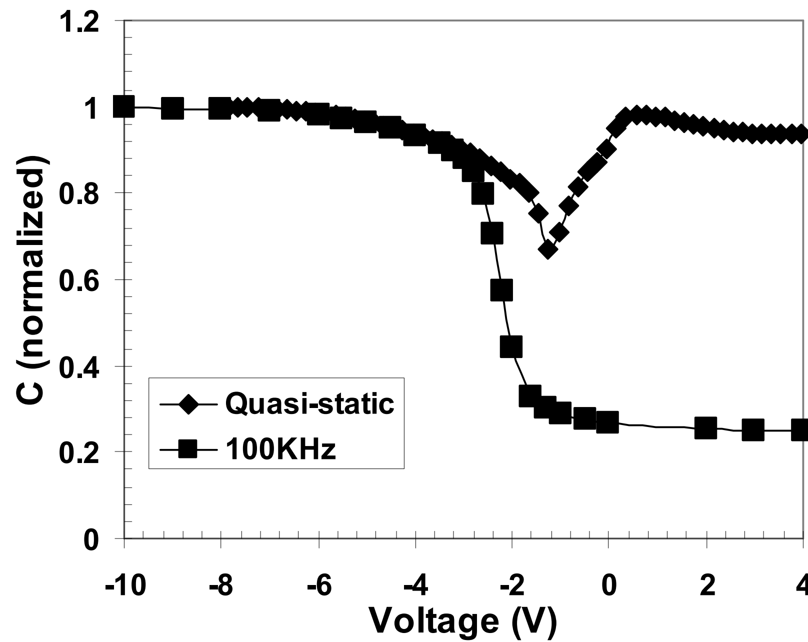

Figure 4.4 Normalized C-V plot for defect density estimation in PECVD oxide

From the above figure we find that C_{HF} = 0.24C_i, and C_{LF} = 0.62 C_i. Using the above equation, we calculate the defect density of our PECVD oxide as 2.82×10^{11} $cm^{-2}eV^{-1}$. This value of defect density is reasonably low for comparable values reported in the literature, indicating that we have been able to deposit a high quality oxide by PECVD. The defect density however, is large compared to thermal oxides and there is a considerable scope for reducing this defect density either by a different deposition scheme, particularly by ECR-CVD or through proper annealing and passivation.

4.6 PECVD Nitride defect density

The C-V characteristics for our best PECVD silicon nitride sample is shown in figure 4.4 below. This nitride was deposited at a pressure of 400mTorr, a power density of

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75mW/cm^2 with $N2O/SiH_4$ and He/SiH_4 ratios of 20 and 100 respectively. A more detailed discussion follows in the chapter on nitrides.

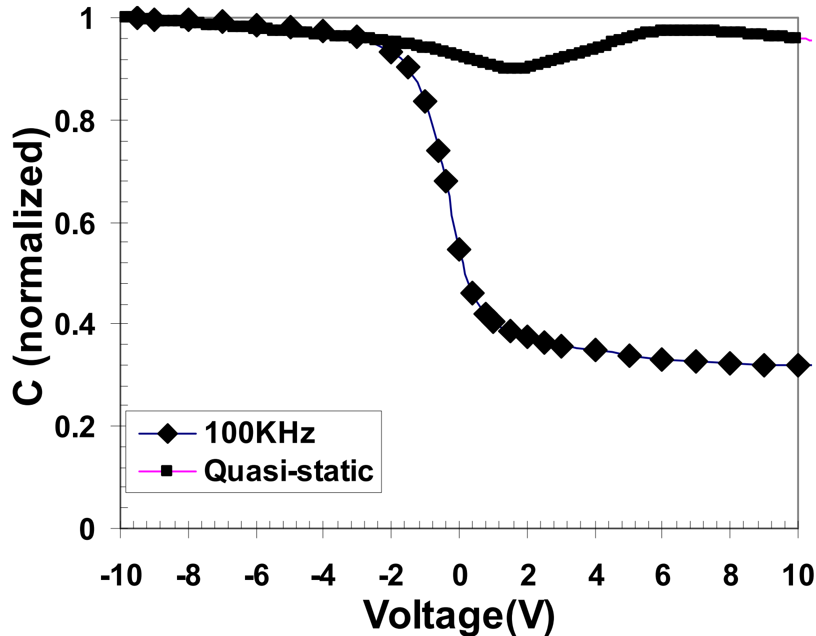

Figure 4.4 Normalized C-V plot for defect density estimation in PECVD nitride

From the above figure we find that $C_{HF} = 0.26C_i$, and $C_{LF} = 0.82$ Ci. Using the same, we calculate the defect density of our PECVD silicon nitride as 7.72×10^{11} $cm^{-2}eV^{-1}$.

It is important to note that the defect density of silicon nitride is considerably higher than our PECVD deposited silicon dioxide, and is expected. For this reason, we decided to use silicon dioxide as our gate dielectric in this work. Nevertheless, silicon nitride has a better leakage performance and can be used in a gate dielectric stack with oxide to have both low defect density and low leakage in addition to acting as a diffusion barrier to hydrogen. To conclude, we have developed both high quality oxides and nitrides during the course of this work which can be put to appropriate use in future depending upon the need.

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CHAPTER 5. PECVD SILICON NITRIDE

5.1 Introduction

Amorphous silicon nitride (a-SiN_x:H) deposited by plasma enhanced chemical vapor deposition is widely used as passivation layers in conventional semiconductor processing, and also as gate dielectric in thin film transistors for large area electronics. For devices fabricated on glass substrates, the deposition temperature has to be below 500°C, and good quality silicon nitride has already been achieved in these temperature ranges [33]. But, for devices to be compatible with flexible substrates and organic light emitting diodes, reduction in deposition temperature to 300°C and less is a primary requirement. The challenge therefore is to develop a material with good dielectric performance at such low temperatures. Despite this, some research groups have reported successful fabrication of a-Si:H TFTs using PECVD silicon nitride [33-35], with a gradual improvement in device performance [36].

For meeting the requirements of a gate dielectric in thin film transistors, the a-SiN_x:H material should be capable of withstanding high electric fields (~3MV/cm) without breaking down. In addition, it should have a low density of electronic traps, a low rate of charge trapping at lower electric fields, and a high quality interface with the semiconductor material. A survey of literature reveals that for optimal TFT performance, such as high field effect mobility and low charge injection into the nitride under gate bias stress, nitrogen rich a-SiN_x:H ($x>1.33$) has to be used [37,38]. Such films possess a high band gap with a low trap density, and high breakdown strength. In this chapter, we report

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on the growth and properties of a-SiN_x:H films deposited by RF-PECVD at 300°C using a mixture of ammonia, silane, and helium as source gases.

5.2 Silicon Nitride Growth

Silicon nitride was deposited using a parallel plate RF-PECVD reactor at a frequency of 13.6MHz, and is described in a previous section. The source gases used were silane, ammonia, and helium with the substrate temperature being set at 350°C. The actual substrate temperature was around 75°C–100°C less than indicated. The total gas pressure and the gas constituents were varied to study the respective effects on growth of the film.

During plasma deposition of N-rich a-SiN_x:H from silane and ammonia, aminosilanes $Si(NH_2)_{n\leq 4}$ have been identified to be the primary precursors of growth [39] from mass-spectrometry studies. The aminosilane molecules are formed in the gas phase from silane and ammonia radicals. This reaction mechanism is different from that using SiH_4 and N_2, where no Si-N precursors are formed in the gas phase, and the Si-N bonds are established in the film. NH_3 has higher dissociation energy than SiH_4, and so the formation of ammonia radicals requires higher electron energy in the plasma as compared to the formation of silane radicals. Therefore, to create an excess of ammonia radicals, a high plasma power and a high ratio of ammonia to silane is required [40]. It is under these circumstances only that a large majority of silane radicals get nitrided and prevent the formation of Si-Si bonds in the film, which otherwise result in poor electronic properties.

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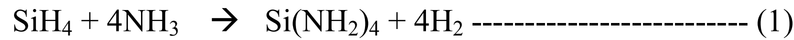
5.3 Reaction Mechanism

Under optimal conditions, all silicon species are fully nitrided and yield tetra-aminosilane according to [41]:



$$SiH_4 + 4NH_3 \rightarrow Si(NH_2)_4 + 4H_2 \text{ ------------------------- (1)}$$

This gas phase reaction shows the abstraction of four hydrogen atoms from a silane molecule and their replacement by NH_2 groups.

$Si(NH_2)_4$ molecules gets adsorbed on the film surface with a low sticking coefficient and promotes the growth of a dense and compact film [41]. The next step of the reaction is followed by ammonia abstraction resulting in a-SiN_x:H and proceeds as [41]:

$$3Si(NH_2)_4 \rightarrow Si_3N_4 + 8NH_3 \text{ ----------------------------- (2)}$$

This reaction occurs at the surface or subsurface of the growing film, whereby NH_2 groups are split off from the Si atom forms NH_3 molecules by reacting with H from nearby N-H bonds. The NH_3 molecules leave the growing film surface once they are formed. During this process, the Si and N atoms can cross-link, and the efficiency of this process depends upon the substrate temperature. For this reason at high temperatures both N and H content of the film is reduced, while at low temperatures three hydrogen atoms can be expected to be incorporated for each excess N atom.

5.4 Silicon Nitride Deposition Considerations

For realizing a high quality dielectric material, we studied the effects of pressure and reactant gas dilution ratios on the electrical and structural properties of silicon nitride films. The films were deposited in a parallel plate RF-PECVD reactor as described above with a plasma power density of $75mW/cm^2$. This power density was found to be

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appropriate for achieving both high dissociation of ammonia, and a moderate growth rate for dense films. PECVD silicon nitride films which are nitrogen rich exhibit better electrical properties [39]. To promote nitrogen incorporation in the film, we increased the ammonia fraction in the gas mixture using NH_3/SiH_4 ratios of 15, 20, and 25 respectively.

A hydrogen/silane ratio of 6 was used in depositing some silicon nitride films under the assumption of better passivation of the dangling bonds. These, films however showed a high leakage current, probably due to the presence of Si-H bonds, and the use of hydrogen was therefore discarded. To promote better ion bombardment, a He/SiH_4 ratio of 75 was used in these runs. The beneficial aspects of using a high helium dilution would be covered in detail in the chapter on oxides.

5.5 Spectroscopic Analysis

To find out the optimized deposition parameters for silicon nitride gate insulators, we prepared a series of films with varying flows of ammonia and silane at different pressures and keeping the temperature constant at 300°C. To reduce the sample preparation time, the breakdown strength of films deposited under varying chamber pressure were first evaluated using a MIM structure (to be discussed in a following section). The films prepared under an optimal pressure of 400mT were then characterized from their FTIR spectra to study the effect of NH_3/SiH_4 ratio.

The FTIR spectra of the series of films are shown in the following figure 5.1. The absorption peaks in the spectrum correspond to well known vibration modes [43], and are typical of a silicon nitride film.

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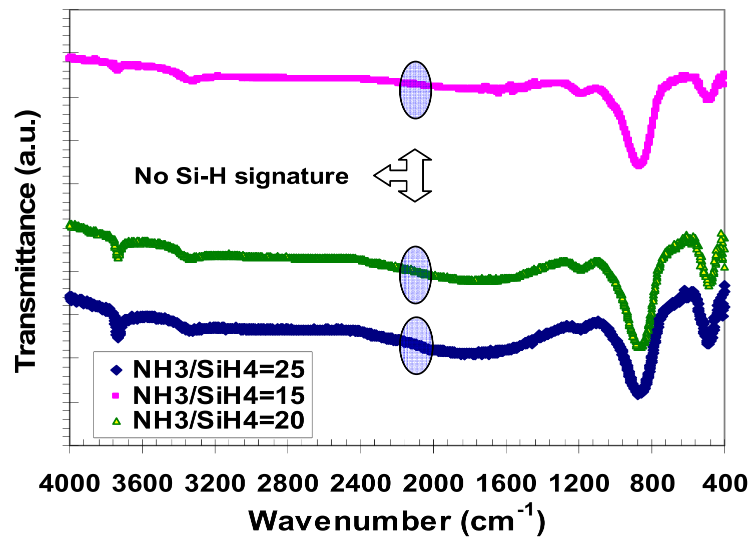

Figure 5.1 FTIR spectra of silicon nitride

The highest peak at around 800cm^{-1} corresponds to Si-N stretching mainly in the NSi_3 configuration, and the shoulder at 1180cm^{-1} represents the bending mode. The peak at 1550cm^{-1} is due to NH_2 bending. The contributions due to SiH_n and NH stretching appear at 2180cm^{-1} and 3340cm^{-1} respectively. A small shoulder at 3450cm^{-1} corresponds to NH_2 stretching.

It has been shown that silicon nitride films deposited with NH_3/SiH_4 ratio R$\leq$ 30 are inert to the absorption of moisture and are dense [43]. We find that with increasing R, the SiN mode in the FTIR spectra gets smaller. This can attributed to a lower Si-N bond density, and are thus indicative of a less dense material. The hydrogen in the film gets predominantly bonded to N, and we do not see the Si-H bond signature in the FTIR spectra. This is indicative of a good film, as the Si-H bonds can contribute to leakage and can also result in drift of threshold voltage over time due to gate bias induced degradation. We chose a NH_3/SiH_4 ratio of 20 for our gate dielectric as an optimal

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compromise between achieving a nitrogen rich film and a film which is inert and thus stable in the long-run. The deposition pressure was varied between 100mT and 500mT, and the nitride film with best properties was attained at a deposition pressure of 400mT. Higher deposition pressure promotes better gas phase decomposition and the films are dense. Too high a pressure results in unwanted gas phase reactions and particle formation. The growth rate also increases with pressure and a high growth rate leads to poor quality film. The following table summarizes some of the selected results.

Table 5.1: Deposition conditions and properties of SiN_x films grown at 15MHz RF and 300°C

Power	Pressure	H_2/SiH_4	NH_3/SiH_4	He/SiH_4	g.rate	V_{BD} (MV/cm)	Defect Density
12W	100mT	----	25	75	80Å/min	2.09	N.A.(leaky)
9W	100mT	----	25	75	65Å/min	2.12	N.A.(leaky)
5W	100mT	----	25	75	55Å/min	2.89	1.11×10^{12} $cm^{-2}eV^{-1}$
5W	100mT	6	25	75	50Å/min	1.56	N.A.(leaky)
5W	100mT	----	15	75	48Å/min	3.18	9.83×10^{11} $cm^{-2}eV^{-1}$
5W	100mT	----	20	75	51Å/min	3.81	8.72×10^{11} $cm^{-2}eV^{-1}$
5W	400mT	----	20	75	60Å/min	5.21	7.72×10^{11} $cm^{-2}eV^{-1}$
3W	400mT	----	20	75	54Å/min	4.52	7.48×1011 $cm^{-2}eV^{-1}$

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5.6 Electrical Transport in Silicon Nitride

Transport in SiN_x thin films is generally discussed in terms of three mail transport mechanisms which are as follows:

5.6.1 Ohmic conduction

Silicon nitride films exhibit an ohmic region at low electric fields. Under low applied fields, the number of generated carriers is determined by the temperature. These trapped electrons or thermally excited carriers hop from one localized stare to the other leading to ohmic J-E characteristics given by Mott and Twose [38] as:

$$J_{OH} = C_{OH} E \exp(-\beta \Phi_{OH}) \text{ --------------------------------------- (1)}$$

where J_{OH} is the current density, C_{OH} is the pre-exponential parameter, E is the electric field, $\beta = (K_B T)^{-1}$, K_B is the Boltzmann constant, T is the absolute temperature and Φ_{OH} is the thermal activation energy.

5.6.2 Frenkel-Poole conduction

This mode of conduction occurs typically at high fields and high temperatures. This process is usually strongly temperature dependent. The Frenkel-Poole conduction is described by the following equation:

$$J_{FP} = CE \exp [(-q/K_B T)\{ \Phi_B - (qE/\pi\varepsilon_o\varepsilon_d)\}] \text{ ------------------ (2)}$$

where, C is a constant determined by the trap density, Φ_B is the Frenkel-Poole barrier height, and ε_o and ε_d are respectively the permittivity of free space and the insulator dielectric constant.

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5.6.3 Fowler-Nordheim conduction:

This occurs typically at high fields and low temperatures, due to tunneling of carriers over a triangular barrier. The current density J_{FN} resulting from tunneling by the Fowler-Nordheim mechanism given by Weinberg [44] is:

$$J_{FN} = C_{FN}E^2 \exp(-E_{FN}/E) \quad (3)$$

where, the pre-exponential parameter C_{FN} is inversely proportional to the barrier height (Φ) of the nitride, and the exponential parameter, $E_{FN} \propto (\Phi)^{3/2}$.

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CHAPTER 6. PECVD SILICON DIOXIDE

6.1 Introduction

Silicon nitride has been the gate insulator of choice for active matrix liquid crystal displays using thin film transistors of hydrogenated amorphous silicon. This is because silicon nitride deposited by plasma enhanced chemical vapor deposition at 300°C and at a frequency of 13.6MHz is reasonably stable, forms a good interface with a-Si:H, and the TFTs are only n-type [45]. However, the rather small valence band offset with Si and wide valence band tail makes nitride a less good insulator for holes [46]. Silicon dioxide, on the other hand has a large band gap of 9eV and presents a large barrier for both electrons and holes. For this reason, low temperature silicon dioxide has become very attractive as gate material in flexible CMOS device applications involving polycrystalline and nanocrystalline silicon. Silicon dioxide has excellent material properties and forms a good interface with Si. Also, the trapping probability in SiO_2 is several orders of magnitude lower than Si_3N_4 and a significantly smaller mechanical stress.

Historically, PECVD oxides are porous. These oxides exhibit more pinholes, a lower breakdown electric field and larger trapping state densities than thermally grown oxides [47]. There have been numerous attempts to develop acceptable low temperature PECVD SiO_2. Batey and Tierney [48] have shown the need to use low growth rates by studying low temperature PECVD deposition. Lucovsky et al.[49] have developed a sub 900°C process for conventional CMOS using a remote plasma, as an alternative to thermal oxide [50]. Many authors have compared various precursors such as silane or

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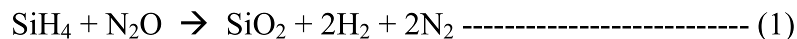
tetra-ethoxy silane and O_2 or nitrous oxide (N_2O) including Yuda et al. [51]. Over the past decade, there has been a considerable effort to produce SiO2 films by ECR, by various groups including Herak et al. [52], Andosca et al. [53], and others [50, 54].

6.2 Deposition Mechanisms

The reaction of conventional PECVD SiO_2 without He dilution is given by [63].



$$SiH_4 + N_2O \rightarrow SiO_2 + 2H_2 + 2N_2 \text{ --------------------------- } (1)$$

Without any dilution, reactive gases easily fracture uncontrollably where virtually the gas phase reactions take over leading to particulates in the reaction chamber. Direct plasma excitation of SiH_4 and N_2O results in several reactive byproducts, including SiH, SiH_2, SiH_3, etc. These species can take part in heterogenous reactions leading to unwanted bonds such as N-H, Si-H, Si-O-H, Si-N, etc. in the deposited films [62].

The precursor molecules for PECVD SiO_2 deposition was identified by Longeway et al. [64] as being the disiloxane [$(SiH_3)_2O$]. The SiH_4/N_2O mixture diluted by He was reported to increase the production of disiloxane precursor by Pai et.al. [62]. The reaction sequence for the deposition can be written as [65]:

$$N_2O + X^* \rightarrow NO + N^* \text{ -------------------------------------- } (2)$$

$$NO + X^* \rightarrow N^* + O^* \text{ -- } (3)$$

where, X* denotes the excited He atoms or excited electrons in the plasma, N* and O* are respectively the excited nitrogen and oxygen atoms.

The excited oxygen atoms react with SiH_4 to produce $(SiH_3)_2O$, and participate in surface reactions to produce SiO_x films. The reaction for producing the disiloxane can be written as [65]:

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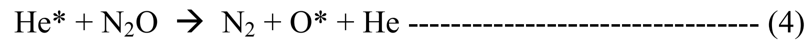
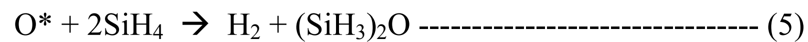
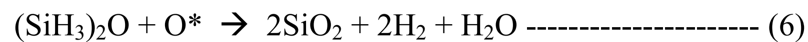


$$He^* + N_2O \rightarrow N_2 + O^* + He \text{ ---------------------------------- } (4)$$



$$O^* + 2SiH_4 \rightarrow H_2 + (SiH_3)_2O \text{ -------------------------------- } (5)$$

The surface reactions involve the elimination of H from the Si-H bonds of disiloxane via a reaction in which the terminal hydrogen atoms are replaced by oxygen atoms [65]. This surface reaction can be written as



$$(SiH_3)_2O + O^* \rightarrow 2SiO_2 + 2H_2 + H_2O \text{ ---------------------- } (6)$$

6.3 Silicon Dioxide Film Deposition

In this work we deposited silicon dioxide from a mixture of silane, nitrous oxide and helium in a Radio-Frequency CVD reactor. At this point it should be noted that we have chosen a low-frequency CVD for depositing silicon dioxide instead of using high frequency CVD. This is because, a higher amount of ion bombardment is necessary for a good dielectric with minimal voids and pinholes, and is unlike the case for nanocrystalline silicon where a high ion bombardment might lead to lattice damage. Thus by choosing a low frequency, we can have a controlled and beneficial amount of ion bombardment which coupled with a lower growth rate at low frequency leads to better oxide quality, as has been described in detail in the chapter on CVD.

In the very beginning of our work on depositing silicon dioxide films by PECVD, we used a mixture of silane, nitrous oxide, and oxygen diluted in helium. The oxygen was supposed to aid in the oxidation of silane in addition to nitrous oxide. Though oxygen has been used by a few groups in depositing silicon dioxide, we have some reservations after doing some initial runs. In fact, we found out that the silicon dioxide film quality was worse for comparable films deposited with and without the use of oxygen. A possible and

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logical reason for this is the fact that oxygen reacts explosively with silane producing dust. This dust formed inside the reaction chamber can get incorporated within the film leading to non-uniformities and voids resulting in poor electrical characteristics.

6.4 Spectroscopic Analysis of SiO_2 Films

We performed Fourier Transformed Infrared Spectroscopy (FTIR) measurements on selected RF-PECVD deposited silicon dioxide films, since they provide the most direct information about the local bonding environment of constituent atoms. For FTIR measurements, SiO_2 films of the same thickness were deposited on double polished crystalline silicon wafers after a piranha clean and buffered oxide etch. The following figure shows the FTIR spectra of two SiO_2 films deposited at 300°C, with He/SiH_4 ratio of 200 and N_2O/SiH_4 ratios of 30 and 50 respectively at incident power of 50mW/cm^2 at 13.6 MHz RF.

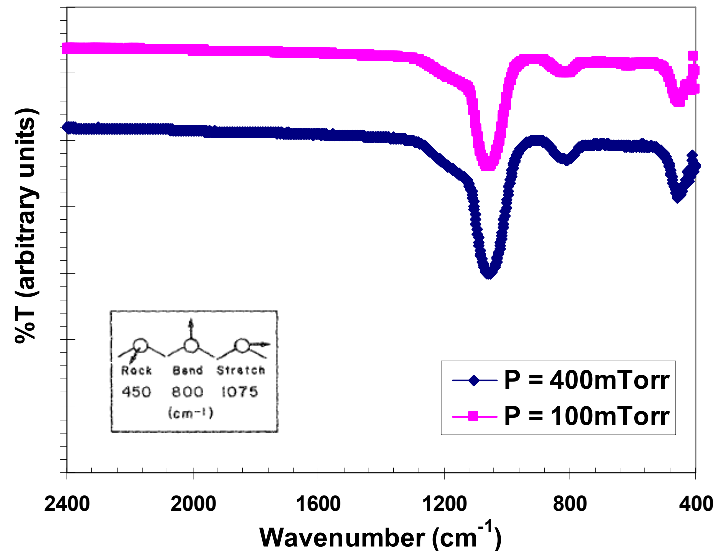

Figure 6.1 Estimation of alloy composition from FTIR spectra of PECVD silicon dioxide films

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There are three characteristic bands for SiO_2 occurring at frequencies of approximately 1075cm^{-1}, 800cm^{-1}, and 450cm^{-1} and respectively correspond to stretching, bending and rocking motions of the twofold coordinated oxygen atoms [49]. It has been shown [62] that the frequency of the stretching band bears a linear relationship with $SiO_x(x<2)$ alloy composition from about 940cm^{-1} for low concentrations of oxygen in a-Si to about 1075cm^{-1} in stoichiometric SiO_2. In our films, the stretching vibration has frequencies of 1071cm^{-1} and 1065cm^{-1} at deposition pressures of 400mTorr and 100mTorr respectively. These correspond to an x-value ≈2 in SiO_x implying that we have been able to produce close to stoichometric silicon dioxide. Note that at deposition pressure of 100mTorr, the stretching band peak drifts away (1065cm^{-1}) from the stoichoimetric peak of 1075cm^{-1}, while at 400mTorr this peak (1071cm^{-1}) approaches that of thermal oxides. Moreover, the absence of Si-H vibration modes in our FTIR spectra confirms that the deleterious hydrogen bonds are at a minimum and limited by the resolution of the FTIR instrument.

6.5 MOS Capacitors in Nanocrystalline Silicon

When silicon dioxide is deposited by PECVD to form MOS capacitors with nanocrystalline silicon as the semiconductor material, the leakage current increases by orders of magnitude over the corresponding MOS capacitors fabricated using Si-wafers. The breakdown strength of the oxide decreases appreciably, and fails even at low electric fields of 10^5V/cm. Also, due to the high leakage current, the MOS capacitors were very unstable and even high-frequency C-V measurements were not possible. A critical investigation into the cause of this failure led us to believe that hydrogen from

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nanocrystalline silicon could be the possible reason. More so, because the oxide were sufficiently thick to discount any effect caused by the roughness of the substrate. The experimentally observed oxide breakdown for both crystalline silicon and nanocrystalline silicon MOS capacitors are shown below for comparison.

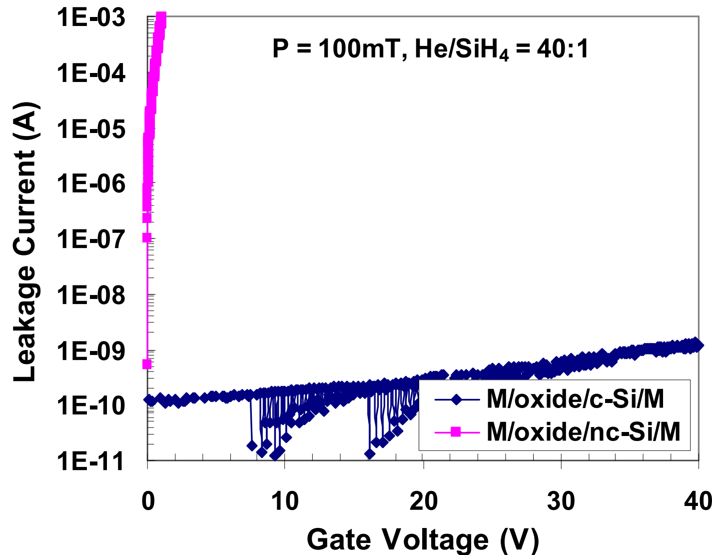

Figure 6.2 Illustration of breakdown problem in nc-Si:H MOS capacitors

6.6 Hydrogen in Low Temperature SiO_2

At low deposition temperatures, the electrical properties of SiO_2 deteriorate because of the role played by hydrogen and the presence of SiOH and SiH groups. Hydrogen has many beneficial and detrimental properties in Si based materials.

Hydrogen passivates the Si dangling bonds thereby removing the gap states and improving electronic properties in hydrogenated amorphous silicon. However, the mobility of hydrogen under electronic excitation is the reason for electrical instability, such as the Stabler Wronski effect and bias stress instabilities in TFTs [55]. In silicon dioxide, hydrogen passivates the dangling bonds at the Si/SiO_2 interface [56]. But, Si-H

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bonds form states within the SiO_2 gap, and so they are unstable to carrier trapping or electronic excitation [62]. The hydrogen released from interface Si-H bonds when broken by hot carriers is mobile and can react with other defect sites [58, 59].

The O-H bond is also unstable to charge trapping in bulk SiO_2, where it is a precursor of the non bridging oxygen [60]. OH groups can also be present as interstitial water molecules and are likely to be quite mobile in SiO_2. It is therefore important, that the presence of both Si-OH and Si-H groups be minimized, particularly the Si-H bonds. Though the hydrogen content of PECVD silicon dioxide can be quite less than silicon nitride, but is more deleterious because of the wider gap and lower network density of SiO_2 [61].

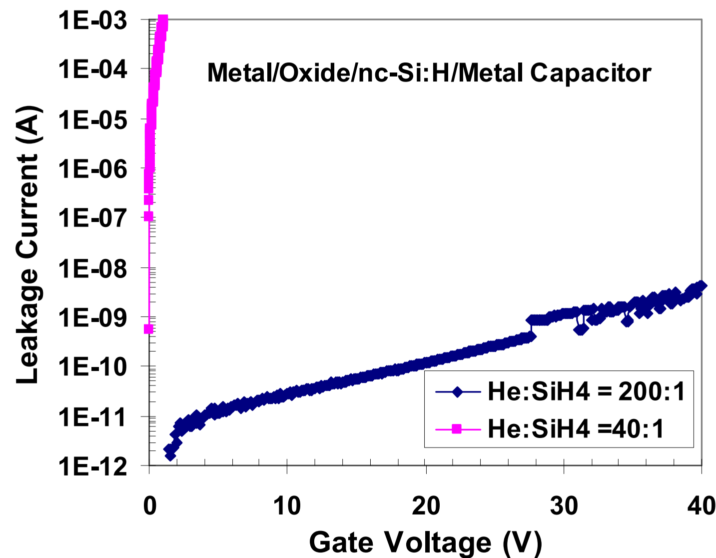

Figure 6.3 Illustration of the role of helium dilution in reducing breakdown

6.7 Role of Helium Dilution

During deposition of PECVD SiO_2, it is important that the growth rate be sufficiently low so as to produce a more dense film with minimal pinholes and voids. For

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this reason helium is commonly diluted with silane so as to effectively decrease the amount of SiH_4 in the reaction while maintaining a large flow through the mass flow controller for accuracy. Whether helium provides any beneficial role at high temperature (>400°C) depositions of oxide is debatable, but at low temperatures, it is almost a necessity as we and others [66] have found out. A direct effect of a higher helium dilution is evident from figure 6.3, where an increase in He/SiH_4 dilution ratio from 40 to 200 has resulted in a leakage current reduction through the oxide deposited over nanocrystalline silicon by about seven orders of magnitude.

In the helium dilution approach, we use a rather high flow of helium for diluting the reactant mixture consisting of silane and nitrous oxide (N_2O). Ion bombardment can be minimized during deposition since helium is light, inert and clean. Helium has the best thermal conductivity, and is capable of suppressing the unwanted gas phase reactions which results in a greater surface uniformity and less powder formation. Moreover, helium has a large cross section for excitation of energetic electrons which helps in igniting and maintaining the plasma.

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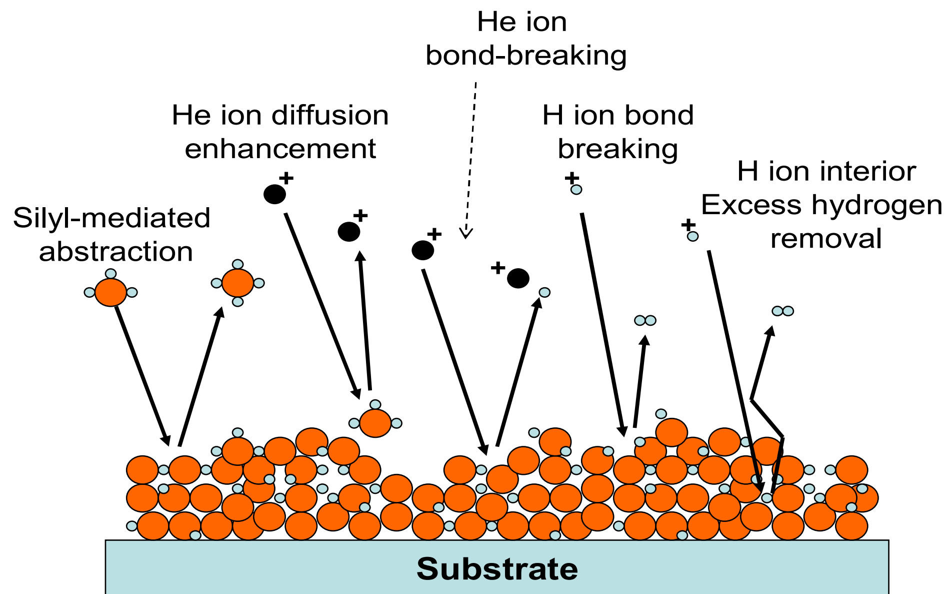

Figure 6.4 Schematic of ion bombardment mechanism using helium dilution [67]

Importantly, at low substrate temperatures, helium ions provide the necessary momentum for surface mobility of species, effectively compensating for the thermal loss. Helium dilutions are capable of reducing unwanted Si-H, Si-OH, Si-N, N-H etc., which have been confirmed by Fourier Transform Infrared Spectroscopy [62]. These hydrogenous bonds, as discussed in the previous section, degrade the performance of PECVD oxide and reduce its density. Helium also enhances tendency towards stoichiometric composition by exciting oxygen to form SiO_x films.

6.8 Deposition Pressure and Oxide Leakage

To study the effect of chamber pressure on the electrical characteristics of RF-PECVD oxides, a set of two oxide films were grown at 100mTorr and 400mTorr respectively.

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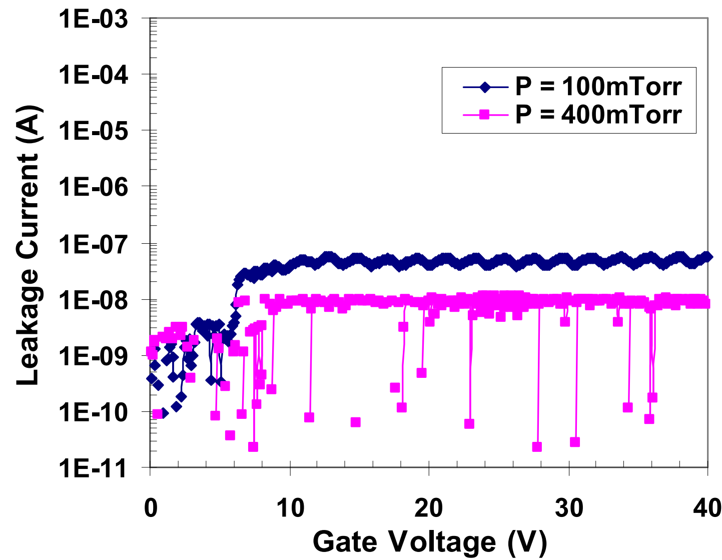

Figure 6.5 Influence of deposition pressure on electrical properties of PECVD oxides

From the above figure, we find that for the same thickness of oxide (~1100Å), the film deposited at 400mTorr exhibited a significantly lower amount of leakage as compared to the film deposited at a lower pressure of 100mTorr. This can be explained by the fact that at higher pressures, the film decomposition is more uniform due to a higher amount of ionization of gas molecules. Note that the growth rate also increases as pressure goes up, and so does the possibility of unwanted gas phase reactions.

A delicate balance therefore has to be achieved for having both high quality film and minimum particulate formation by optimizing the deposition pressure. In our case, we found that a chamber pressure of 400mTorr leads to films with overall better characteristics.

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CHAPTER 7. HIGHLY CONDUCTIVE DOPED FILMS

7.1 Introduction

Recently there is a considerable interest in the growth of hydrogenated nanocrystalline silicon at low substrate temperatures with emphasis on low cost and flexible plastic substrates for application to large area and roll-roll production of thin-film transistors, photovoltaic and optoelectronic devices [68-71]. Hydrogenated nanocrystalline silicon has been shown to be much better than hydrogenated amorphous silicon in terms of device stability under light soaking in solar cells and gate bias stress in thin film transistors, in addition to possessing higher mobilities and lesser defects. Particularly, highly phosphorous doped and boron doped nc-Si:H have been shown to have much higher conductivities and better doping efficiencies than their amorphous counterpart. For these reasons, p^+ nc-Si:H contacts for solar cells and thin film transistors are expected to provide low series resistance and better quality ohmic contacts.

Doping of amorphous silicon was demonstrated by Spear and Lecomber [72], Kanicki et al [73], He et al [74], and Kuo and Latzko have demonstrated highly conductive n^+ uc-Si:H as source/drain contacts in a-Si:H TFTs. For optimized deposition conditions (T_{sub}>200^oC), room temperature dark conductivities are generally above 10^{-3}S/cm for p-type films [75,76]. Doped nc-Si:H films deposited above 200^oC have optimized conductivity of 40S/cm for p-type films [77].

In this work, we discuss the improvement in conductivity and crystallinity of p-type nanocrystalline Si:H layers by the use of post-deposition annealing. The p layers

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were deposited at ~ 180°C from mixtures of silane, hydrogen, helium and diborane using ECR plasma deposition techniques. It was found that addition of He to H at first improved both the conductivity and crystallinity, but too much He led to an amorphous phase and lower conductivity. The as-grown films were measured for their crystallinity using both Raman spectroscopy and x-ray diffraction. The conductivity and activation energies were also measured. The films were then successively annealed at temperatures of 250°C, 300°C, 350°C, and 400°C. The crystallinity and grain size were found to increase as the annealing temperature increased. The greatest relative increase was during the initial annealing stages. The conductivity of the films increased significantly as a consequence of the annealing. Conductivities as large as 20 S/cm were obtained in very thin films (~50nm-150 nm). The corresponding activation energies were in the range of 0.03 eV. When these annealed layers were used for MOSFET and PV devices, there was an appreciable increase in performance characteristics.

7.2 Film Preparation

The p^+ nc-Si:H films were deposited by ECR-PECVD in a deposition system described elsewhere [78]. Corning 7059 glass and double-side-polished c-Si wafers were used as substrates. The vacuum base pressure before actual deposition was ~10^{-7} torr. A 10 min hydrogen etch followed by a 40 min dummy of a:SiC:H with ppm TMB was done to reduce any oxygen introduced in the chamber while loading the sample. All depositions were done at a pressure of 5-6mT and at temperatures indicated. The ratio of diborane over silane was varied between 6% and 31% to find out the optimal doping ratio for an optimal hydrogen dilution of 99.7%. Then hydrogen and helium dilutions were

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varied keeping the optimal doping ratio as fixed. Hydrogen dilution is defined as $F_{H2}/(F_{SiH4}+F_{H2})$ ×100% and helium dilution as $F_{He}/(F_{H2}+F_{He})$×100%. The total flux was kept constant between 80sccm and 85sccm.

7.3 Film Characterization

p^+ nc-Si:H films deposited on 7059 Corning glass substrates were used for Raman, XRD, and electrical measurements. Selected p^+ films were deposited on double polished c-Si wafers for FTIR measurements. The thickness measurements were performed using a Perkin-Elmer lambda 9.

For electrical measurements, coplanar Cr contacts 20mm long, 1mm apart, and 1000Å thick was evaporated through a shadow mask in a thermal evaporator under a vacuum pressure of ~10^{-7}torr. The dark conductivity σ_d was measured at room temperature. The activation energy E_a was calculated from $\sigma_d = \sigma_0 \exp(-E_a/K_bT)$

Raman Spectra for crystallinity in the backscattering geometry was measured using a Renishaw Raman microscope. To prevent thermally induced crystallization, the incident laser beam power was kept below 50mW. The peaks were deconvoluted and the crystalline volume fraction was deduced from the integrated Raman intensity ratio $X_c = (I_{520})/(I_{520}+\eta I_{480})$, where I_{520} and I_{480} are the deconvoluted intensities of the Raman spectra in crystalline (520cm^{-1}) and amorphous (480cm^{-1}) peaks, respectively, and η, the scattering factor, was 0.8 [79]. The film structure was investigated using a grazing incidence XRD measurement. The average grain size was was found out using the Scherrer formula [80].

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7.4 Conductivity and Hydrogen Dilution

Figure 7.1 shows the dark conductivity and crystallinity as a function of boron doping with 99.7% hydrogen dilution, grown at 200°C with B_2H_6 as the doping gas. As the B_2H_6/SiH_4 ratio is varied between 6% and 30%, we find that the conductivity initially remains fairly insensitive between 8% and 12% of B_2H_6 over silane, and the crystallinity remains essentially the same. Then as we increase the diborane flow, the crystallinity decreases while the conductivity reaches a maximum at around 59% C.F. After this the conductivity and crystallinity drops off sharply with increasing diborane leading to an amorphous material.

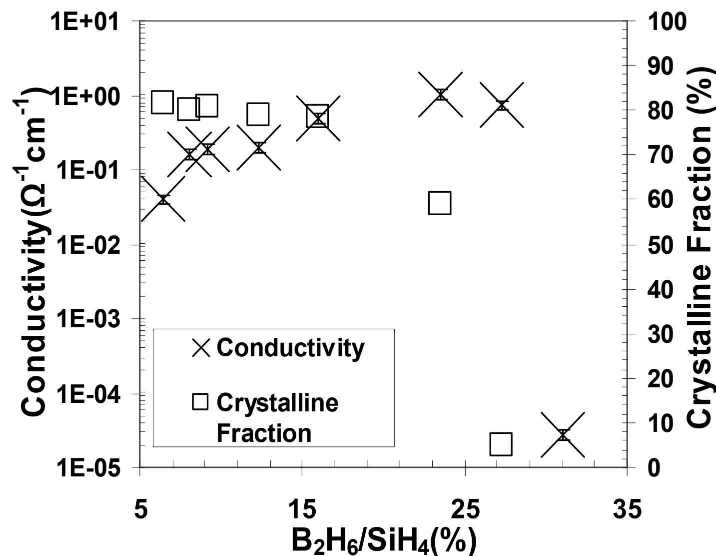

Figure 7.1 Variation of conductivity with B_2H_6/SiH_4 ratio at 99.7% H.D

As the B_2H_6/SiH_4 ratio is varied between 6% and 30%, we find that the conductivity initially remains fairly insensitive between 8% and 12% of B_2H_6 over silane, and the crystallinity remains essentially the same. Then as we increase the diborane flow, the crystallinity decreases while the conductivity reaches a maximum at around 59% CF.

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After this the conductivity and crystallinity drops off sharply with increasing diborane leading to an amorphous material.

This is an interesting result as the highest conductivity occurs in a mixed phase material, wherein we can tune the bandgap depending upon the application and still not compromise much in conductivity. All previous work reported so far has focused only in the 0.5% to 1% diborane doping regime and lower hydrogen dilutions [75,76]. The reason we can have a comparatively wide doping window without compromising much in crystallinity is our relatively larger hydrogen dilution of 99.7%. For a film prepared with 99% H_2 dilution, the crystallinity remains essentially the same, but is accompanied by a sharp drop in conductivity as compared to an otherwise similar film prepared with 99.7% H_2 dilution as shown in figure 7.2.

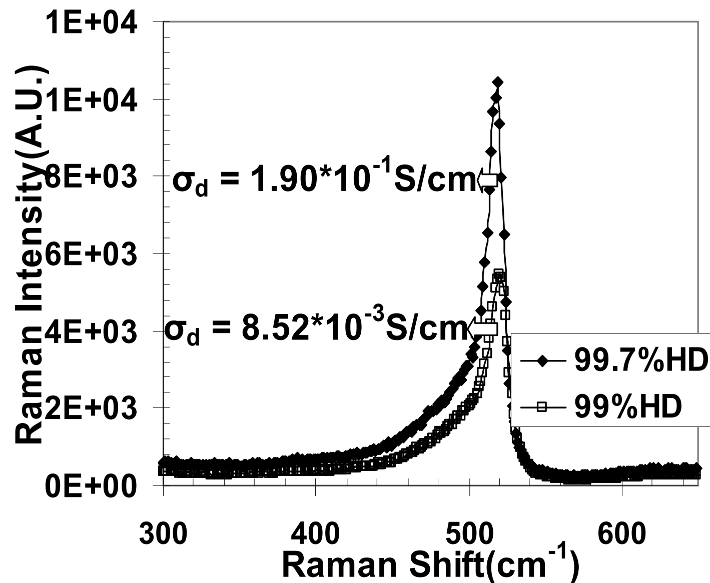

Figure 7.2 99% H.D. vs 99.7% H.D. Note the drop in σ_d at 99% H.D.

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7.5 Hydrogen and Helium Dilution

Figure 7.3 shows the change in conductivity and crystallinity when the deposition temperature is reduced from 200°C to 150°C. We find that though the change in conductivity is not appreciable, the crystalline fraction drops significantly from 81% to 64%.

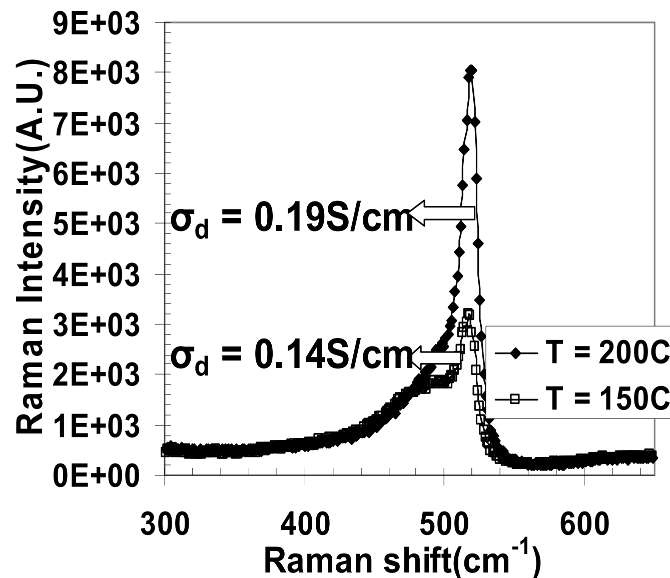

Figure 7.3 Effect of growth temperature reduction on conductivity and crystallinity

By increasing hydrogen dilution, or reducing the diborane concentration, we can improve the crystallinity further, but a corresponding increase in conductivity could be limited by the passivation of boron atoms by hydrogen which become increasingly pronounced at lower deposition temperatures [75,81]. Moreover at lower temperatures, the concentration of defects (dangling Si bonds) increases, the concentration of di- and polyhydride-bonded hydrogen in the films increases, the mass density decreases, leading to poor film quality [16].

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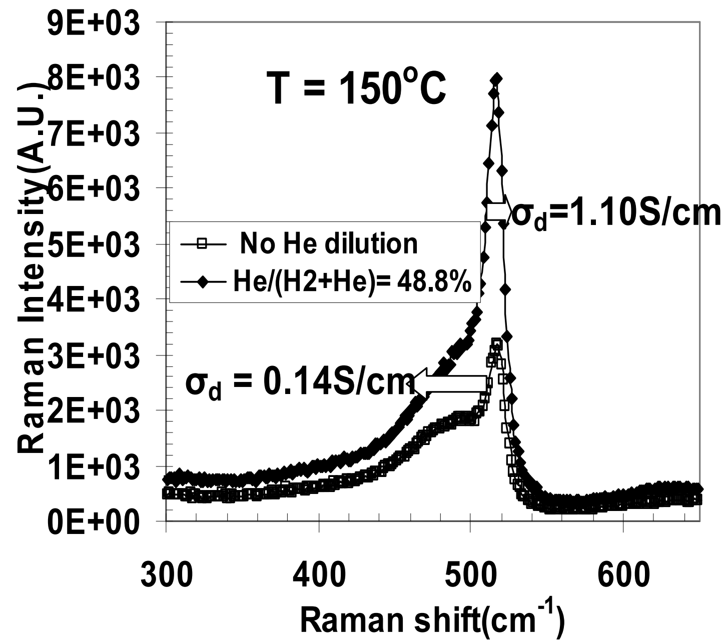

Figure 7.4 Improvement in σ_d and crystallinity upon He dilution at lower temp.

It is widely known that presence of He in the plasma can affect the energy distribution mechanisms mainly through the He metastable species [71]. Also, addition of He causes activation of surface processes by very mild ion bombardment without damaging the material structure. Particularly, at low substrate temperatures, mild helium bombardment can compensate for the thermal energy loss and improve film quality [71]. Figure 7.4 shows the relative improvement in crystallinity and conductivity for a film prepared using both He and H_2 dilutions as compared to a corresponding film with only H_2 dilution.

Figure 7.5 shows the variation of conductivity and crystallinity with He dilution shown as a percent of the total dilution, which has been kept constant at 99.7% with respect to silane. The B_2H_6/SiH_4 flow ratio is kept fixed around 9%.

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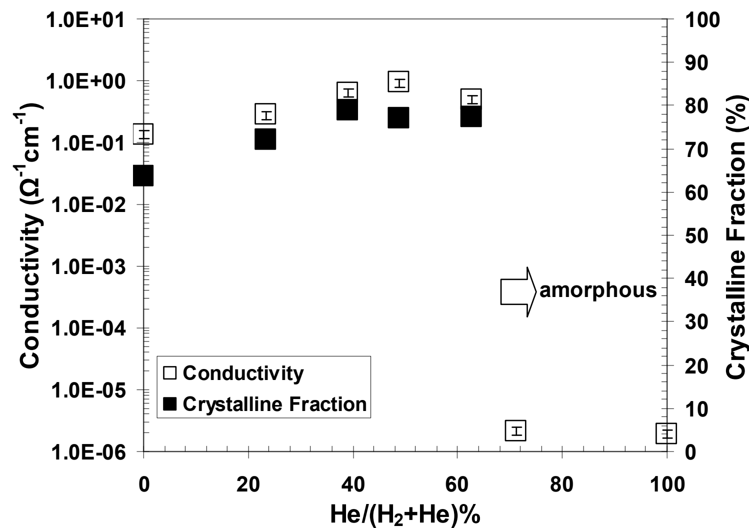

Figure 7.5 Effect of He dilution in addition to hydrogen dilution

We observe that as the He dilution is increased, the conductivity and crystalline fraction improves. This continues and reaches a peak at around 50% helium dilution, where the conductivity is about an order of magnitude higher than the corresponding sample without any helium dilution. As we increase the He dilution further, the conductivity drops off, and after 65% He dilution, the rate of decrease is significantly faster with the sample turning into amorphous with orders of magnitude reduction in conductivity. The reason behind this is that a larger amount of helium in the plasma destroys the lattice resulting in a highly disordered material.

7.6 Thickness Dependence of Conductivity

Figure 7.6 shows the variation of conductivity and crystallinity as a function of film thickness. Within the range shown we observe an appreciable increase in conductivity as the thickness of the film increases from 65nm to 150nm.

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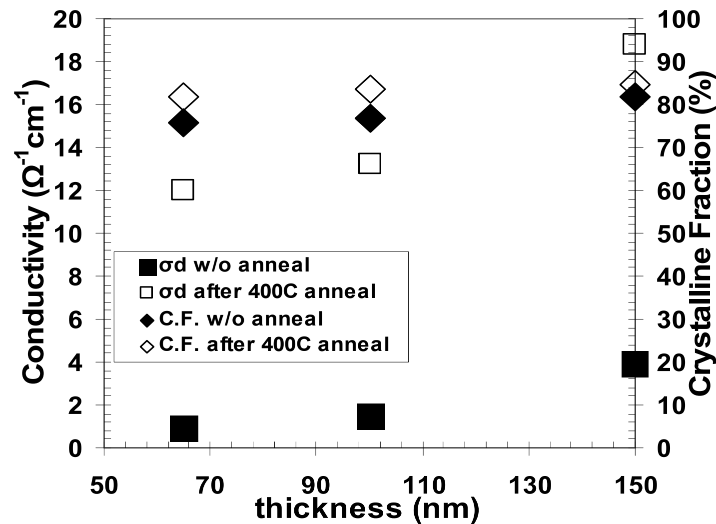

Figure 7.6 Conductivity and crystallinity as a function of thickness and anneal.

The crystalline fraction of the film also improves as we go to higher thickness. The crystallinity and conductivity are expected to saturate after a certain thickness [71], and we have not probed beyond 150nm as this is supposed to be the maximum thickness for most device applications [70,71]. The grain size as determined from X-Ray diffraction was in the range of 20nm-25nm, while the activation energies were around 0.03eV, showing an increasing trend with decreasing conductivity.

7.7 Annealing Experiments

We present the results of annealing of some selected films in figures 7.6, 7.7, and 7.8. The samples were annealed in increments of 50°C in a nitrogen atmosphere starting from 250°C and ending at 400°C. The dark conductivity and Raman spectra were measured after each annealing step.

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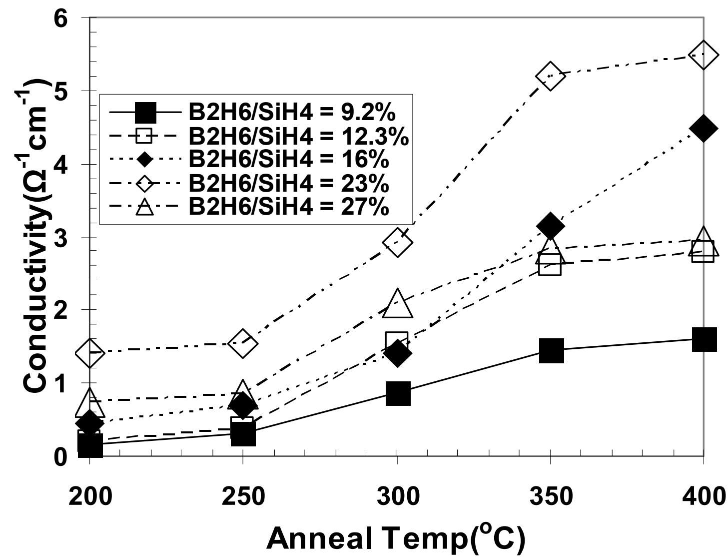

Figure 7.7 Effect of anneal on films deposited at 200°C with 99.7%HD

For the films in figure 7.7, the deposition temperature was 200°C with 99.7% hydrogen dilution and with varying boron over silane ratio as indicated. Figure 7.8 shows the effect of anneal on conductivity for samples grown with varying He dilution and a fixed B_2H_6/SiH_4 ratio of 9.2% at 150°C.

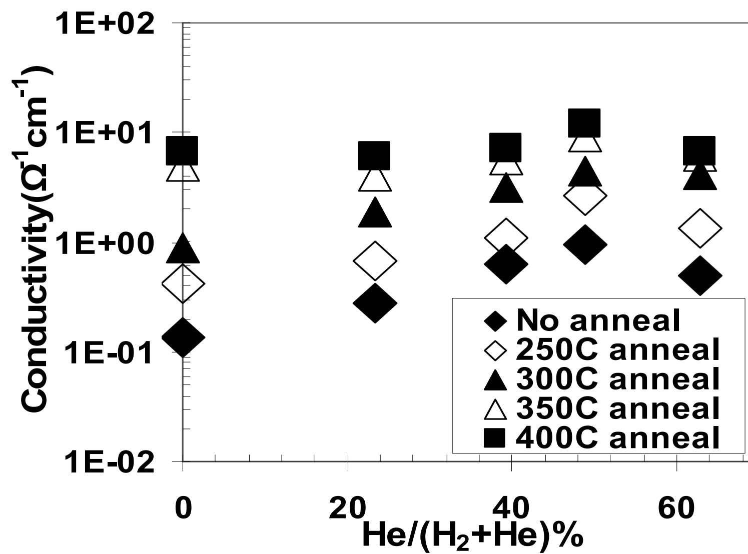

Figure 7.8 Effect of anneal on films deposited at 150°C with B_2H_6/SiH_4 = 9.2%

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For the nc-Si samples with low doping ratios we find that the relative increase in conductivity over anneal was not quite significant as compared to the nc:Si samples with high boron concentration which were amorphous. For nc-Si:H films the conductivity had increased by 8-10 times, whereas the amorphous type films showed an increase in conductivity by about two orders of magnitude. The relative increase in conductivity however was the largest in the initial stages of annealing.

7.8 Discussion

We have investigated the growth and properties of p+ nc-Si:H at temperatures of 150°C - 200°C by ECR-CVD. The conductivity and cyrstallinity of films deposited at a temperature of 200°C and 99.7% hydrogen dilution were studied as a function of the doping ratio.

It was found that the conductivity and especially the crystallinity of the film prepared at 150°C to be poor as compared to a similar film prepared at 200°C. Helium dilution was then introduced to improve the surface activation processes and reduce passivation of boron by hydrogen. The effect of helium and hydrogen dilution was then studied at an optimal doping ratio, which was kept fixed. A high conductivity of 1S/cm and a high crystalline fraction of 77% could be obtained for a film only 60nm thick. We have also shown that the conductivity increases with thickness reaching a value of 4S/cm for a 150nm thick film.

Annealing experiments on the films revealed that the improvement in conductivity was much more in amorphous as compared to nanocrystalline films. The maximum conductivity for a 150nm thick film rose from 4S/cm to around 20S/cm after a

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400°C anneal in nitrogen ambient for 1 hr. This can be attributed to the passivation of a relatively large number of defects in the amorphous phase at lower anneal temperatures and formation of a crystalline material at anneal temperatures nearing 400°C.

In conclusion, we have developed adequately conducting and crystalline boron doped nc-Si:H for device applications to temperatures as low as 150°C. For even lower temperatures more research is needed for a better performance, which we believe can be achieved by adjusting the helium and hydrogen flows in an appropriate amount.

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CHAPTER 8. TFT CHARACTERIZATION

8.1 Introduction

The performance of the nc-Si:H TFTs may be characterized by several parameters such as on/off ratio, field-effect mobility (μ_{fet}), and threshold voltage (V_T). In general, the μ_{fet} value of non crystalline silicon TFTs is much lower than that of a crystalline silicon MOS transistor. Therefore, the aspect ratio W/L of the devices must be large in order to obtain reasonable levels of the drain-source current (in the range of 1 μA). Low value of V_T (several volts) is necessary in order to assure the TFTs compatibility with conventional CMOS ICs. The on/off ratio of a thin film transistor provides us with an overall measure of its feasibility in practical device applications. An on/off ratio around 10^6 is a basic requirement for a thin film transistor for display applications. For CMOS type applications, the mobility should also be high in addition to the above requirements of a high on/off ratio with a low sub-threshold slope.

8.2 MOSFET Theory

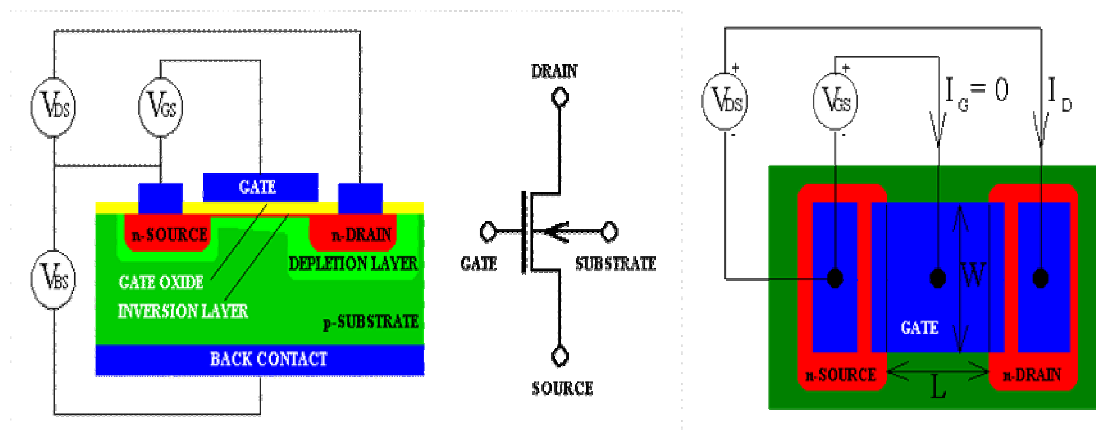

Figure 8.1 Illustration of n-channel MOSFET biasing and dimensions [32]

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According to the theory of the MOSFETs, the transistor enters in saturation regime when V_{DS} is greater than $V_{SAT} = V_{GS}-V_T$. This condition is accomplished when $V_{DS} = V_{GS}$. The following equations for the drain-source current are valid in saturation regime [83].

$$I_{DS} = \frac{W}{L}\mu_{fet}C_{ox}\frac{1}{2}(V_{GS} - V_T)^2 \text{ -------------------------------- (1)}$$

$$C_{ox} = \varepsilon_o \varepsilon_r . \frac{t_{ox}.W}{L} \text{ --- (2)}$$

where μ_{fet} is the field effect mobility, C_{ox} is the gate oxide capacitance, ε_o is the vacuum permitivity, $\varepsilon_r = 3.9$ is the gate oxide relative dielectric permitivity, t_{ox} is the gate oxide thickness, W is the channel width and L is the channel length. The slope of the curve obtained by plotting the square root of the drain current against gate voltage from equation (1) gives us the saturation mobility of the device, and the threshold voltage from the x-intercept.

8.3 Bottom-Gate N-Channel nc-Si:H TFTs

8.3.1 Experimental results

The following figures show the output characteristics of a bottom-gate nanocrystalline silicon TFT with W = 200µm and L = 30µm. The source and drain contacts were Al over n^+ a-Si:H deposited by ECR-CVD and defined by RIE etch. The channel region consisted of an initial a-Si:H layer grown for 2m30s, followed by nc-Si:H deposition with 92.5% H_2 dilution and at a pressure of 100mT. The indicated substrate temperature was 350°C, and the channel was approximately 200nm thick.

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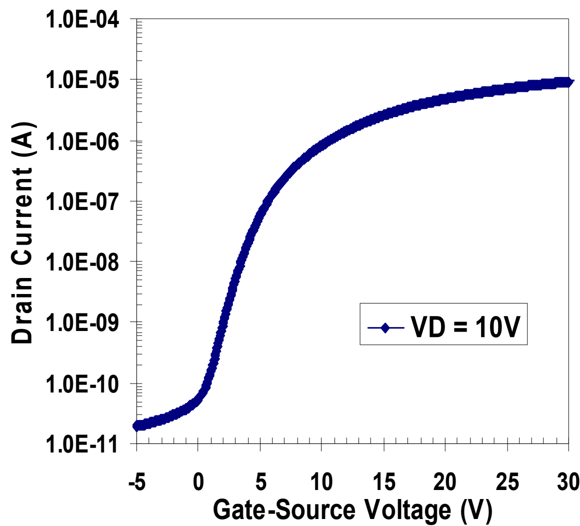

Figure 8.2 Transfer characteristics at drain voltage of 10V with W/L = 200/35

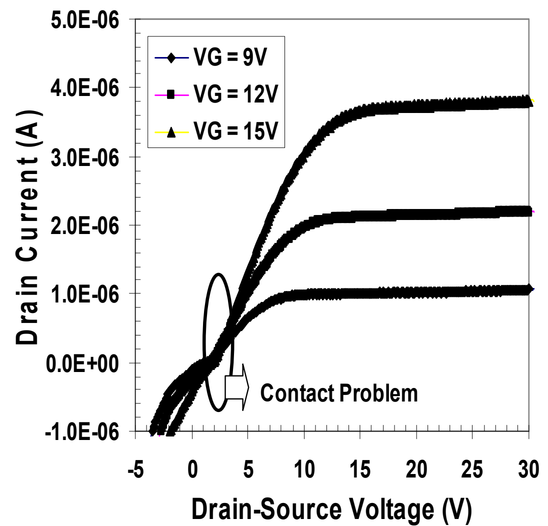

Figure 8.3 Output characteristics for the TFT at varying gate voltages

From the slope of following plot of sqrt (I_D) vs V_{GS}, the value of electron mobility in the saturation region is calculated by a method described in the previous sections.

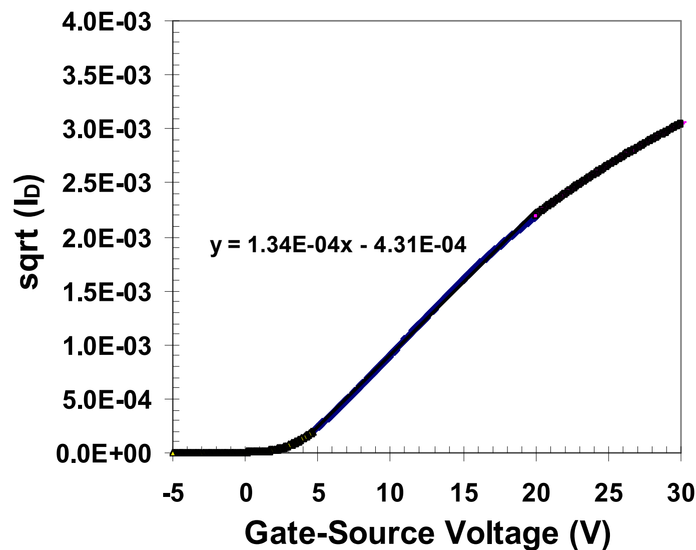

Figure 8.4 Extraction of mobility and threshold voltage with evidence of mobility decrease at high gate voltages

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From the three plots above, the device properties could be deduced as:

$$\mu_n = 0.31cm^2V^{-1}s^{-1} \quad V_T = 3.2V \quad ON/OFF \approx 10^6$$

8.3.2 Discussion

Though the values of threshold voltage and ON/OFF ratio are quite reasonable, the electron mobility at $0.31cm^2V^{-1}s^{-1}$ was quite low, and a value close to $1cm^2/V^{-1}s^{-1}$ was expected.

From the plot of drain current with drain-source voltage, we could clearly see that the curves corresponding to different gate voltages are crowded at low drain-source voltages. This indicates that relatively high resistive contacts are present in the drain and source areas. This observation led us to conclude that the contacts need to improve for a better device performance.

8.3.3 Device with improved contacts

In view of the above observations, a sample identical to the previous one was made using a different parameter for doped layer deposition. The deposition pressure was now reduced and the plasma power was increased so as to make the doped n^+ layer more crystalline. However, a systematic investigation into optimizing this in conductivity and crystallinity was not done due to a lack of time. The following figures show the result of this experiment.

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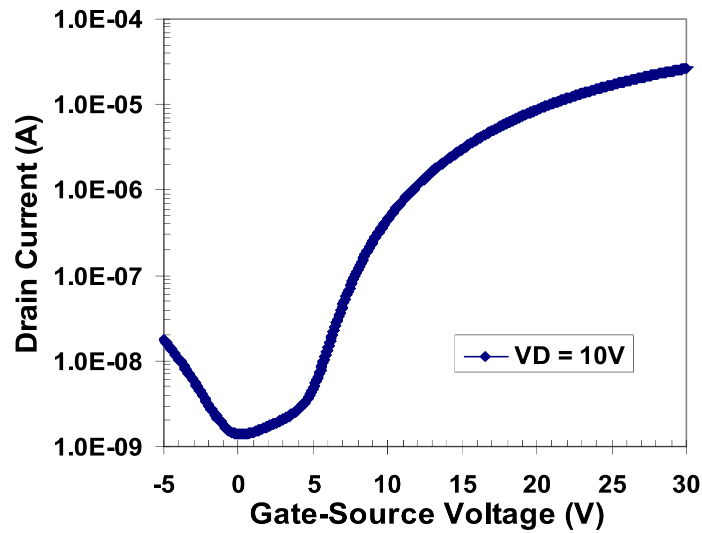

Figure 8.5 Transfer characteristics of the TFT with improved contacts

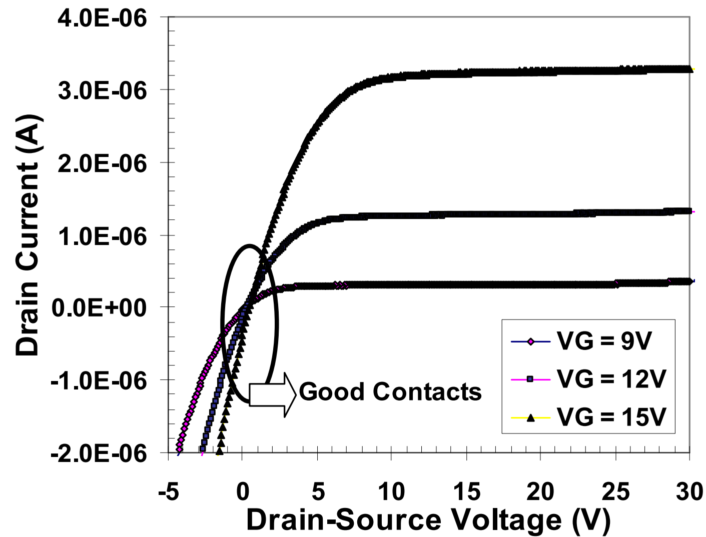

Figure 8.6 Output characteristics of the TFT with no current crowding

This device yielded the following characteristics:

$\mu_n = 0.72 cm^2V^{-1}s^{-1}$ $V_T = 6.5V$ ON/OFF $\approx 5\times10^5$

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8.3.4 Discussion

From the plot of drain-current and drain-source voltage in the second sample, current-crowding is not observed at low drain-source voltages with varying voltage at the gate. We thus conclude that the new n^+ contacts were of better quality and the series resistances were low. For the same channel material, the electron mobility had now increased by over two times.

But this improvement came at a price. The ON/OFF ratio had now decreased by half over the previous sample. The threshold voltage too had increased, but was within the acceptable margin. Ideally, one would expect a better ON/OFF ratio with better contacts as the n^+-p-n^+ double diode should be more effective in preventing carrier flow between the contacts below threshold gate voltage.

The reason for this behavior could be attributed to the doped layer deposition again. Since the pressure was low, and power was high, there was higher ion bombardment, and hence more diffusion of phosphorous into the intrinsic layer, making it lightly n-doped. A direct evidence of this came from RIE etch, whereby, the sample had to be etched for a longer duration to reduce the dark current to a minimum.

8.4 Top-Gate N-Channel TFT

A top-gate n-channel TFT was fabricated with silicon nitride as the gate dielectric. The thickness of the gate dielectric was 250nm. Silicon dioxide deposition was still not device grade by then owing to leakage problems from hydrogen diffusion from the bottom nc-Si:H channel material. The channel deposition parameters were the same as the bottom gate devices. This TFT produced the following results:

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$\mu_n = 0.35 cm^2V^{-1}s^{-1}$ $V_T = 4.1V$ **ON/OFF** $\approx 5\times10^5$

8.4.1 Discussion

The electron mobility from the top-gate device was low as compared to the bottom-gate device shown previously. This is a bit surprising, as the channel layer mobility is supposed to be the maximum at the top. But here, the dielectric was silicon nitride, which had a large number of defects compared to thermal oxide as gate. So the gain in channel layer mobility was now offset by a much more defective dielectric, leading to more scattering of carriers at the interface. Also here, the processing is much more complicated and therefore, a much greater chance of contamination.

Though the device mobility was low, we were still satisfied by the fact that a working device could be fabricated. And since this was the first working device, scope for improvement always remained. A later publication from Arokia Nathan [84] showed a mobility of $0.85cm^2V^{-1}s^{-1}$ with silicon nitride gate dielectric, long after he had demonstrated a mobility of $150cm^2V^{-1}s^{-1}$[85] with silicon dioxide as gate dielectric. With this background, and an improved silicon dioxide, we moved on to fabricating p-channel TFTs as not much has been done in this area.

8.5 Bottom-Gate P-channel nc-Si:H TFTs

8.5.1 Initial results

The first set of devices was made with the same intrinsic nanocrystalline silicon material as the bottom-gate n-channel devices. The doped p+ layer was as usual,

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deposited using remote plasma ECR-CVD with 99% hydrogen dilution with a B_2H_6 to silane ratio at around 26%. The deposition temperature was close to 125°C.

The devices which followed had very poor characteristics. The hole mobility was less than $0.01cm^2V^{-1}s^{-1}$, very high threshold voltages (~-25V) and extremely poor ON/OFF ratios (~10^2).

The first suspect for these problems was attributed to the p^+ contacts. When a similar doped film was made on 7059 substrate, it showed a conductivity of ~ 10^{-5}S/cm, as opposed to 0.22S/cm for a-Si:H n^+ doped layers, and was amorphous. So, a rigorous experiment to improve this was required, and as shown in a previous section, the conductivity could be increased to 1S/cm in only a 60nm thick film.

The following plots show the p-channel TFT achieved with these improved contacts.

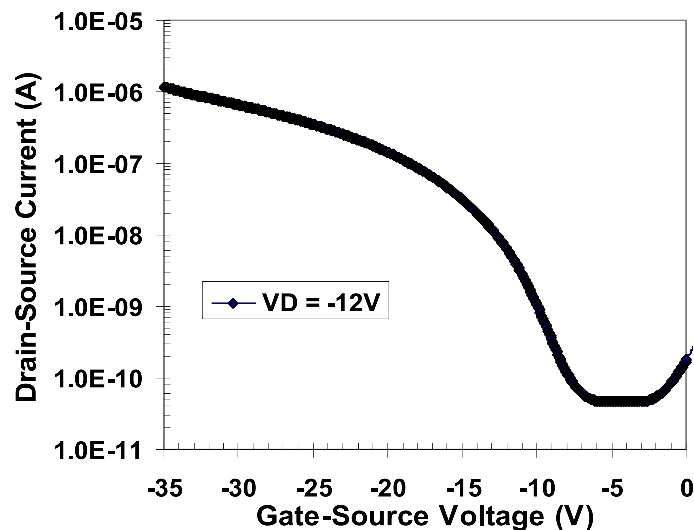

Figure 8.7 Transfer characteristics of our initial bottom gate p-channel TFT

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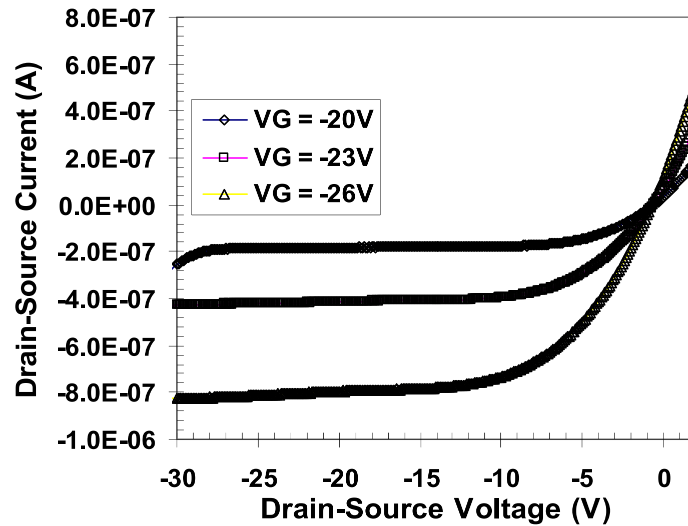

Figure 8.8 Output characteristics of the p-channel bottom gate TFT with better contacts

The gate oxide thickness was 120nm, and device dimensions were W = 200µ and L=40µ

Device results: $\mu_p = 0.048 cm^2V^{-1}s^{-1}$ **$V_T = -10V$** **ON/OFF** $\approx 10^5$

8.5.2 Discussion

As we can see, improvement in contacts led to an increase in hole mobility by about five times, with very reasonable threshold voltage and ON/OFF ratios. Also, there was no evidence of any current crowding, which further confirmed that the contacts were of good quality.

After taking care of the contacts problem, we shifted our focus to improve the nanocrystalline silicon channel layer deposition to improve the mobility. The next section discusses this strategy and the results of the same.

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8.6 Growth Strategy for Channel Material

8.6.1 Bottom gate optimization

For bottom-gate devices, the most critical factor which determines mobility is the interface between the oxide and the nanocrystalline silicon channel. Since the initial layers during nanocrystalline silicon growth are known to be amorphous, it is very essential that good crystallinity is achieved very quickly. It is supposed the effective device mobility is controlled by a very thin region in the channel (~ 20nm) and oxide interface, and as shown in the following schematic, and optimizing this region is our goal.

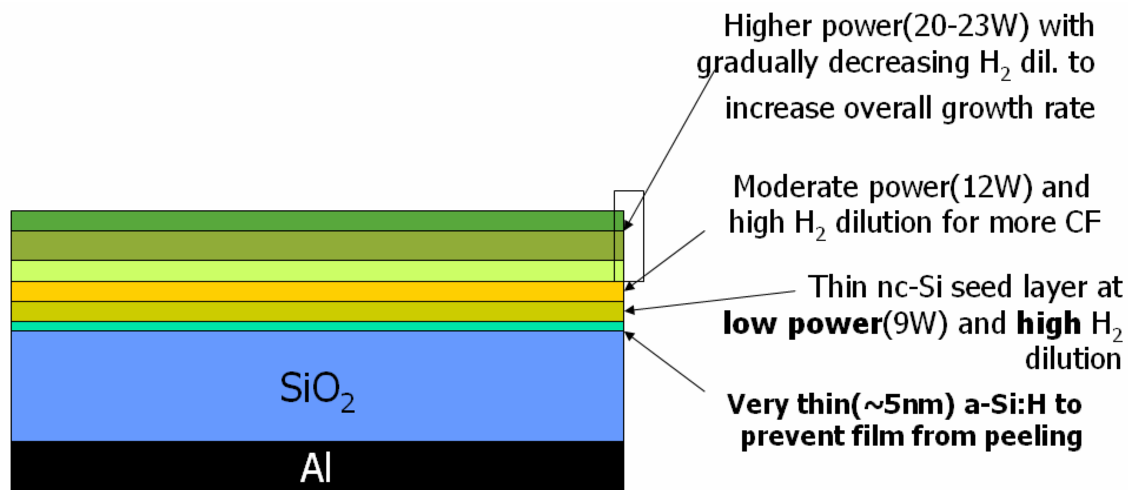

Figure 8.9 Illustration of nc-Si:H deposition scheme for improving mobility

Now, there are some practical problems when to try to reach this idealistic target. Direct deposition of nanocrystalline silicon on top of the oxide leads to peeling off of the film from the surface due to a lot of stress in the nc-Si:H material. Moreover, nanocrystalline silicon deposition involves a high plasma power and thus higher ion

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bombardment, which in turn destroys the crucial oxide interface, resulting in a large number of defects, which are catastrophic to the device performance.

To take care of these problems, the starting film on the oxide is a very thin layer of amorphous silicon, followed by nc-Si:H deposition. However, the thickness of this amorphous silicon layer has to be kept as small as possible, and in the next section we show the improvement in mobility as we progressively make this thinner. Though an ideal thing would be to remove this amorphous silicon layer altogether, we have not met with success so far, and are involved in the process of reducing this to a feasible minimum.

For rapid crystallization, we resort to a very high hydrogen dilution (~99.7%) in the initial nanocrystalline growth phase and at a low power to minimize the deleterious effects of ion bombardment. The growth rate is also kept low to have a more dense structure. Thereafter the hydrogen dilution is reduced and the power increased progressively so as to improve the overall growth rate without compromising on the crystallinity.

The reason for the high growth layers serves two purposes. First, it provides us with a larger margin for RIE etch of the doped p^+ layer on top, and keep the plasma damage from bombardment confined at a safe distance from the oxide interface. Secondly it prevents diffusion of dopant atoms from reaching the channel region, thereby keeping the dark current at reasonable levels.

Having said all this it is also necessary to point out that the channel layer thickness cannot be increased much to avoid collection problems. This requires a fine balance and appropriate adjustments have to be made after troubleshooting.

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8.6.2 Results

The following plots below show the characteristics of the best device obtained from the strategy outlined above.

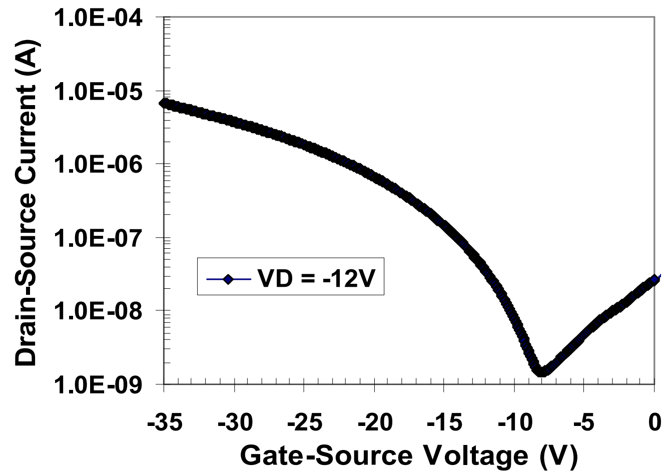

Figure 8.10 TFT transfer characteristics showing drive current improvement

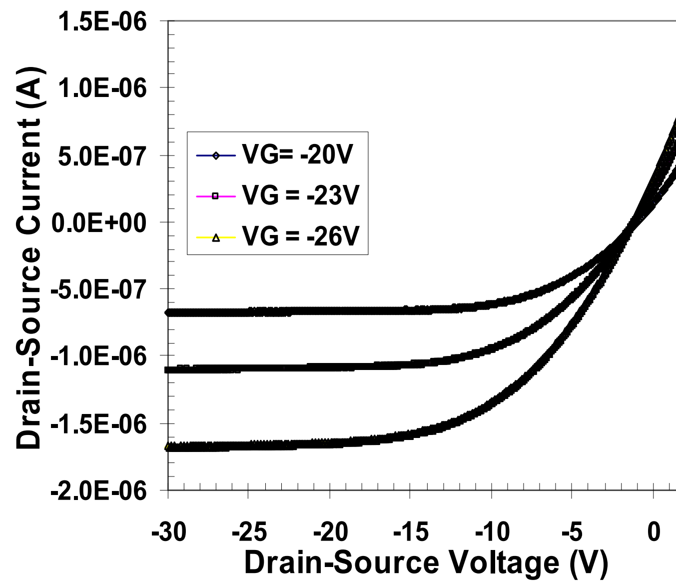

Figure 8.11 Output characteristics of the TFT showing overall improvement

$\mu_p = 0.172 cm^2V^{-1}s^{-1}$ $V_T = -12V$ ON/OFF $\approx 10^4$

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8.6.3 Summary of nc-Si:H deposition

- 2min 30s amorphous, 92.5% H_2 dilution for nc-Si:H at 22W, 100mT

  $\mu_p = 0.048 cm^2V^{-1}s^{-1}$ $V_T = -10V$ ON/OFF $\approx 10^5$

- 1min 30s amorphous, 98.9% HD, low power(9W) at start and graded to 96.6% HD, 22W at end

  $\mu_p = 0.112 cm^2V^{-1}s^{-1}$ $V_T = -12.5V$ ON/OFF $\approx 10^4$

- 1min 30s amorphous, 99.7% HD at start and graded to 96.6% HD at end

  $\mu_p = 0.172 cm^2V^{-1}s^{-1}$ $V_T = -12V$ ON/OFF $\approx 10^4$

8.7 Subthreshold slope

8.7.1 Basic physics

Depending on the gate and source-drain voltages, a MOSFET device can be biased in one of the three regions as shown in the following figure.

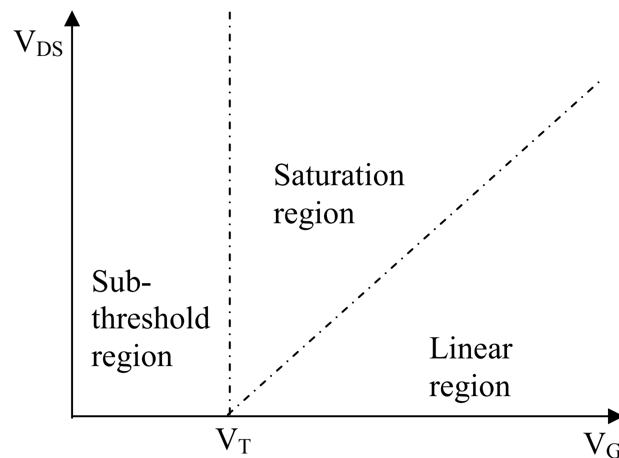

Figure 8.12 Regimes of MOSFET operation [25]

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The linear and saturation regions of MOSFET operation have been discussed above and characteristics of the device in the subthreshold region of operation ($V_G<V_T$) will be the subject of our discussion here. The drain current for $V_G<V_T$ on a linear scale appears to be zero on a linear scale as seen in figure 8.12. On a logarithmic scale, however, this current descends gradually to zero since the inversion layer charge density follows an exponential dependence on V_G and quantified by an inverse sub-threshold slope given by [25]:

$$S = 1/\left(\frac{d(\log_{10} I_{DS})}{dV_g}\right) = 2.3\,\frac{mKT}{q} = 2.3\,\frac{KT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right) \text{---------------} \quad (3)$$

where, I_{DS} and V_G are the drain-source current and gate voltage respectively, K is the Boltzmann Constant, T is the absolute temperature in Kelvin, q is the electronic charge and C_{dm} and C_{ox} are the depletion-layer and oxide capacitances respectively. The value of S is typically 60mV/decade for state of the art crystalline silicon MOSFETS, and can be calculated directly from equation (3) from the experimentally observed I_{DS}-V_G characteristics. Leaving the detailed discussions for a later section, it would be suffice to say that except for a slight dependence on bulk doping concentration through C_{dm}, the subthreshold slope is rather insensitive to device parameters and is only a function of temperature [25].

8.7.2 Experimental characterization

Experimentally, the subthreshold slope can be extracted by performing a linear fit to the logarithmic variation of drain-source current versus gate-source voltage in the

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region below threshold. Figure 8.13 below illustrates this procedure for one of the devices.

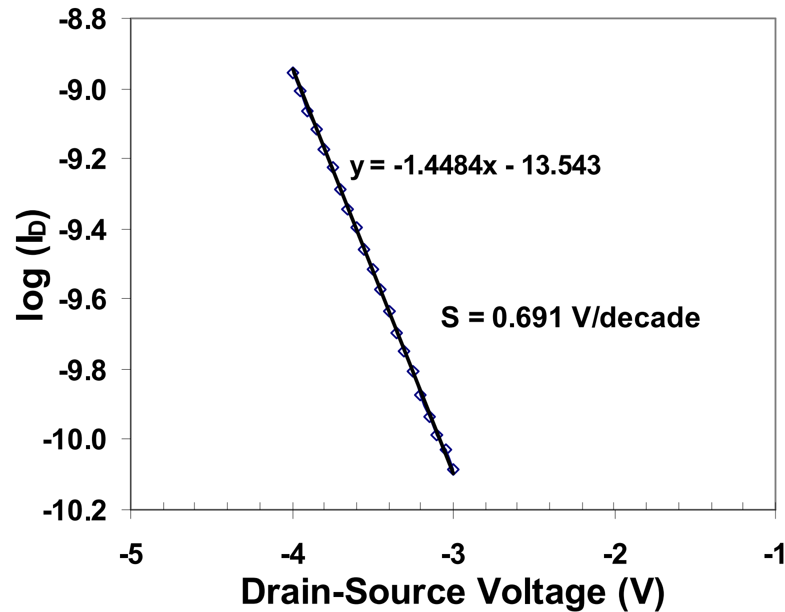

Figure 8.13 Extraction of sub-threshold slope from transfer characteristics

From the above figure, we find the sub-threshold slope for the device from the reciprocal of the slope as 0.691 V/decade.

8.8 High Mobility and Low Leakage Devices

8.8.1 Practical problems

All of the devices discussed above were still suffering from high leakage current in the off state with high threshold voltages. The mobility had improved a lot over the initial devices but was still low for any feasible applications. The above devices provided us with the learning curve that the key to an even higher mobility lies in a careful optimization of the hydrogen dilution to achieve a crystalline material fast enough

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without damaging the oxide interface. As will be discussed below, an even higher hydrogen dilution with low initial VHF power improved the mobility significantly. The high leakage problem was solved by doping the nanocrystalline silicon channel material with ppm levels of phosphine and also by passivating the device with overlayer of silicon dioxide. The threshold voltage could be brought down to lower levels by this novel method of depositing the channel material, ensuring that interface and trap centers are kept to a minimum. In the following sections, we would briefly discuss each of the innovative strategies and their role in improving device performance.

8.8.2 Improved results

Without going into the details and following an approach discussed in the previous sections, the optimized final channel nanocrystalline silicon material deposition parameters with VHF-CVD was as follows:

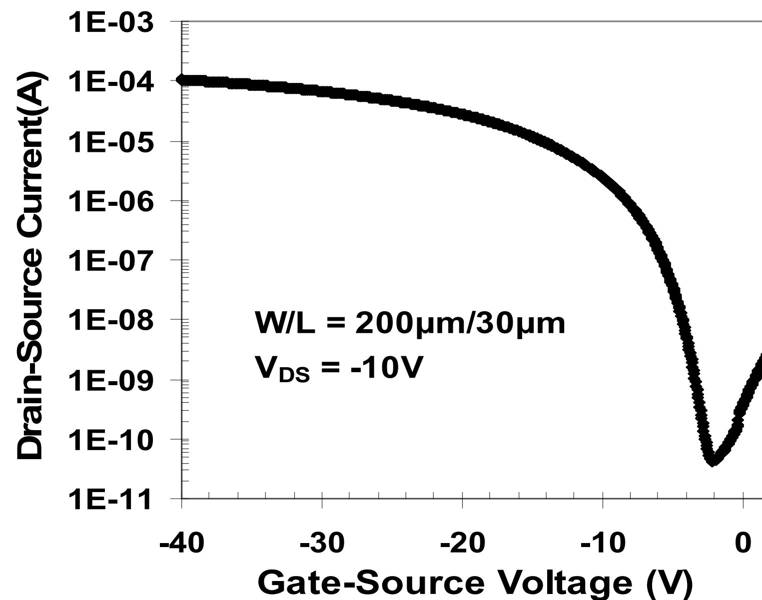

Figure 8.14 Transfer characteristics of a best bottom-gate TFT showing a very high drive current of 0.1mA

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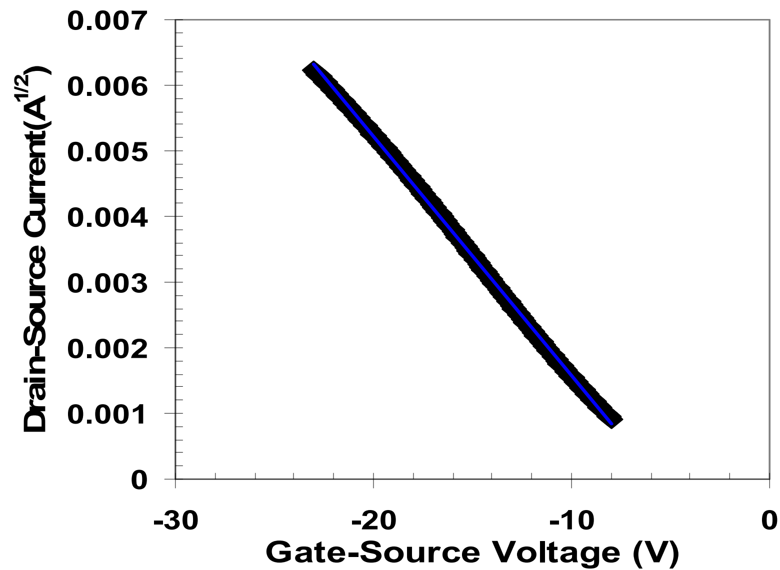

Figure 8.15 Extraction of mobility from square root of drain current as a function of gate voltage

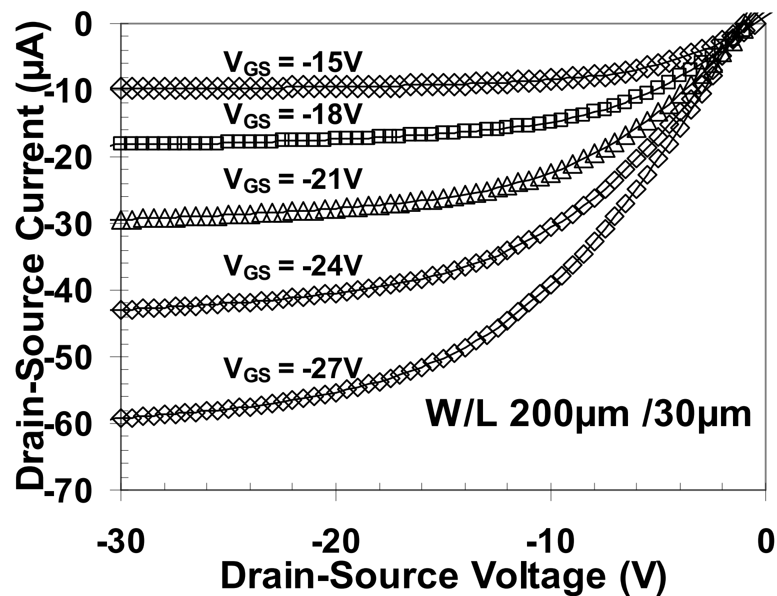

Figure 8.16 Output characteristics of the TFT showing classical MOSFET behavior

From the plot of drain-source current vs drain-source voltage in fig() we find that the TFT followed classical p-channel MOSFET characteristics with no evidence of current crowding at different gate voltages. The reason for this was the highly conductive

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nanocrystalline silicon p^+ contacts which led to minimal contact resistance at the source and drain regions. An important thing to note in this context is the high value of drive current (100μA) achieved in this device with a low threshold voltage as evident from figure 8.14. This is the first time that such a high value of drive current has been achieved in nanocrystalline silicon p-channel TFTs. The mobility and threshold voltage have been extracted from the linear plot of figure 8.15 as discussed in a preceding section. Devices with this recipe showed a high mobility of 1.6 $cm^2/V\text{-}s$ accompanied by a low threshold voltage of -4.5V. This is the best mobility reported so far in literature for similar devices.

8.9 Reduction in Leakage with Channel Doping

8.9.1 Underlying theory

As mentioned above the leakage current in earlier devices was high at around 1nA in the off-state. This coupled with a low mobility led to an ON/OFF ratio of ~ 10^4, which was really low for any practical applications, which necessitate an ON/OFF ratio of 10^6 and above. From classical device physics theory, we know that by increasing the doping in the channel material, leakage through the source and drain junctions are reduced due to formation of stronger reverse biased p-n junctions. This leads to a reduction in the off state current in the device. The penalty that we incur in this process is a reduction in mobility due to impurity scattering. The threshold voltage also increases as we increase the channel doping and is shown in the following figure.

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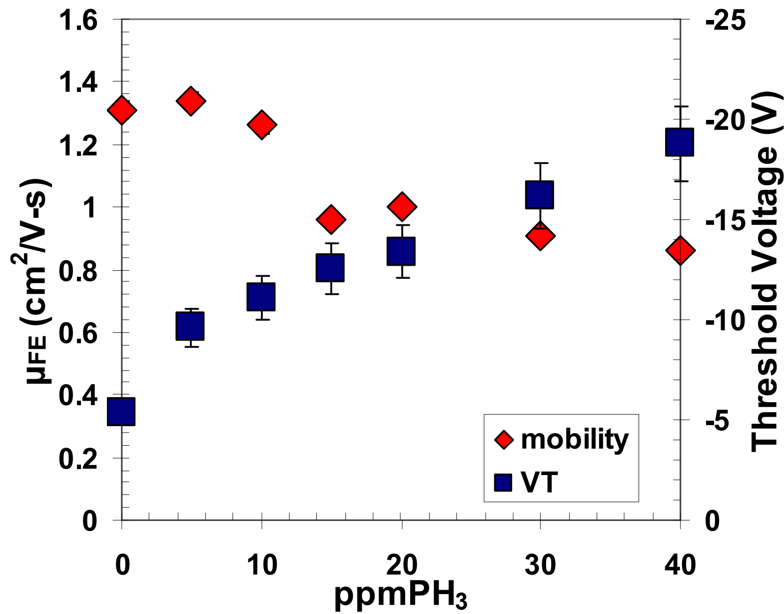

Figure 8.17 Variation of mobility and threshold voltage with channel doping

The increase in threshold voltage with channel material doping (N_D) is given by [83]:

$$V_{TN} = \frac{|Q_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\Phi_{fp} \text{ ------------------------------ } (4)$$

V_{TN} is the threshold voltage for n-channel MOSFET, C_{ox} is the gate oxide capacitance, and $2\Phi_{fp}$ is the surface potential at inversion.

The maximum space charge density per unit area of the depletion region, $Q_{SD}(\max)$ is given by

$$|Q_{SD}(\max)| = eN_a x_{dT} = eN_a \left(\frac{4\varepsilon_s \phi_{fp}}{eN_a} \right)^{1/2} \text{ -------------------------- } (5)$$

where, N_a is the acceptor doping concentration, x_{dT} is the width of the depletion region, and e is the electronic charge.

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From equation (5), we find that the threshold voltage should increase roughly as the square root of doping concentration (N_A/N_D), since the other factors in equation (4) are negligible, and this is indeed the case, as shown in the following figure:

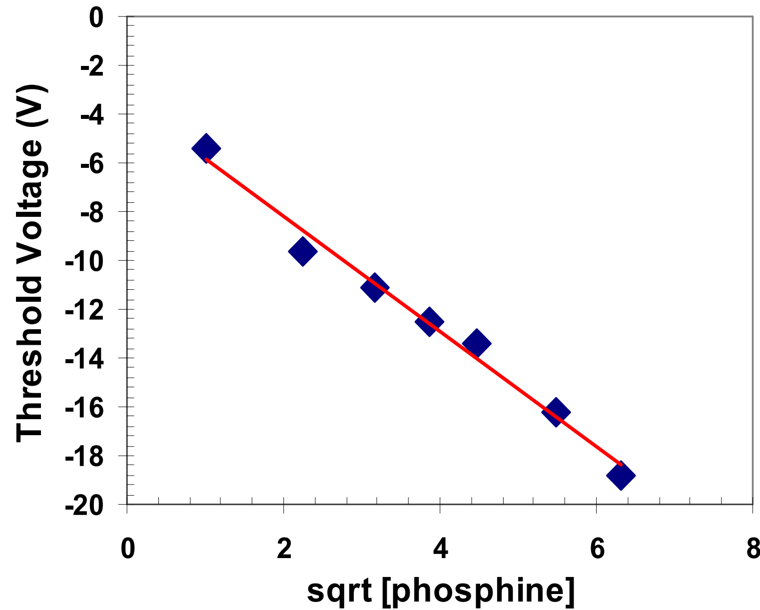

Figure 8.18 Experimentally observed square-root dependence of threshold voltage on body doping of TFT

8.9.2 Experimental results

A closer look into figure 8.17 reveals that the experimental results indeed follow the theoretical predictions. This further tells us about the good reproducibility of devices in between runs as any unintentional doping in the form of moisture remaining in the chamber would have masked this important trend. Great care was taken to ensure the same fabricating conditions by performing 20 minute hydrogen plasma etch to drive moisture out of the chamber before any channel material deposition. Equally important to note is the fact that all previous history of silicon dioxide deposition is eliminated in this process. As a passing note, it may be mentioned that the very high hydrogen dilution used

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in nanocrystalline silicon channel material deposition helped to etch off remaining contaminants.

The following figure shows the effect of ppm phosphine doping on the leakage current and subthreshold slopes for the devices investigated.

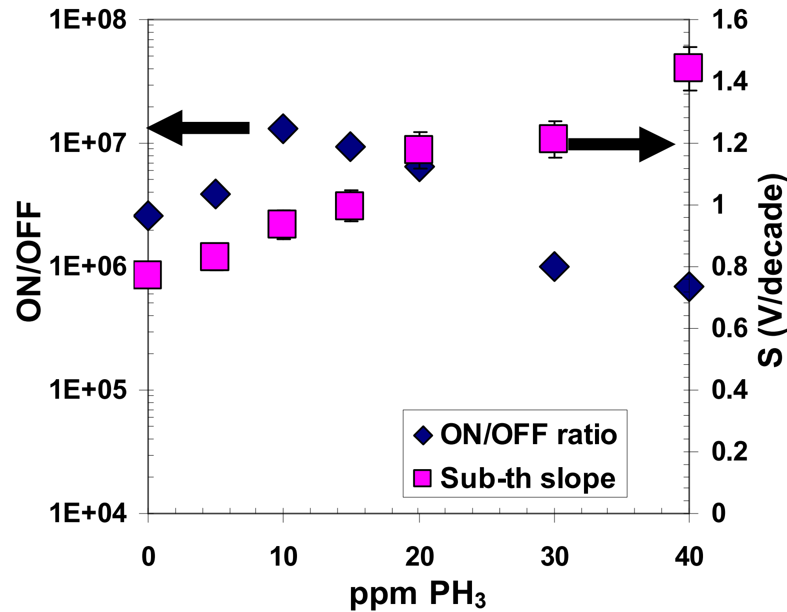

Figure 8.19 Variation of ON/OFF ratio and sub-threshold slope as a function of ppm phosphine doping in the channel

8.9.3 Discussion

From the above, we find that the leakage current decreases with increasing channel doping as predicted, but at higher doping levels (30ppm) the leakage scenario becomes worse. This can be attributed to the recombination current originating from defect centers at the source and drain junctions. The subthreshold slope increases as we increase the doping, and is along expected lines. The minimum subthreshold slope for our device with no doping was around 700mV/decade. This is very high as compared to the ideal subthreshold slope of 60mV/decade, but is lower or comparable to values reported

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in the literature. We don't know the exact reason behind this, but a possible explanation is the presence of a large number of defects inherent in the channel material itself. Also further studies need to be done on improving the nanocrystalline silicon/silicon oxide interface and a solution could lie in passivating the interface defect sites with some special plasma treatment or through annealing.

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CHAPTER 9. TFT FABRICATION BY ALUMINUM DIFFUSION

9.1 Introduction

It is well known that Al behaves as an acceptor state in silicon. Since nc-Si:H is porous as compared to crystalline silicon, it was expected that Al would diffuse into the film when subjected to a low temperature anneal and dope the film p-type. Conventional method of depositing heavily doped nanocrystalline silicon films by in-situ CVD of diborane and silane for source and drain contacts suffers from several drawbacks. Firstly, the film is conformally deposited and requires extra lithography and reactive ion etch steps to define the source and drain regions in addition to the deposition step itself. Secondly, the etch margins have to be appropriately achieved in a small error window to exclude the possibility of overetch or underetch. These assume more significance for CMOS type nanocrystalline silicon thin film transistor devices wherein the level of complexity for putting in this additional layer becomes too high.

In view of the above, we developed a novel method of fabricating nanocrystalline silicon thin film transistors with aluminum diffused source and drain regions, which serve the dual purpose of providing low series resistance contacts by selectively doping the material and also serving as the metal contacts. The method of fabricating the same are outlined below:

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9.2 Aluminum Diffused Diodes

9.2.1 Concept and fabrication

We begin by demonstrating the concept of aluminum diffusion in nanocrystalline silicon by forming a diode structure. The structure of this diode is shown in the following figure:

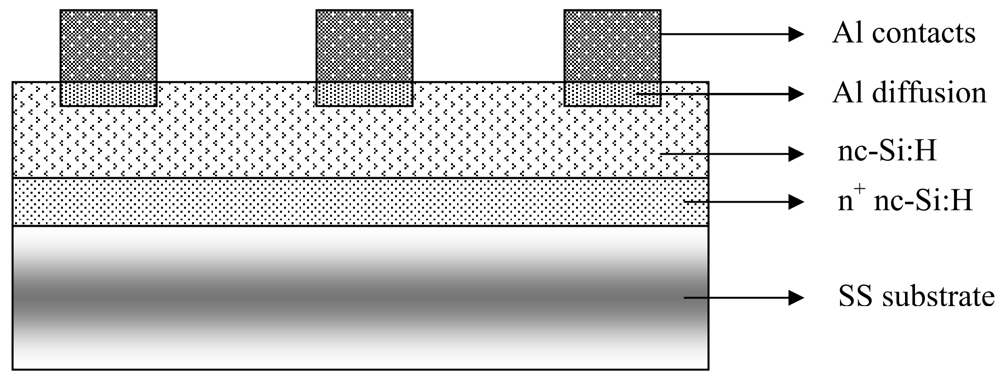

Figure 9.1 Structure of Al-diffused nc-Si:H p-i-n diode

As can be seen from above, the diode is fabricated by depositing a thick layer of heavily doped n-type amorphous silicon film on stainless steel substrates by VHF-CVD. This layer is made amorphous and sufficiently thick (0.4µm) so as to prevent any shorts originating from the surface roughness of the substrate. After this, we grow an undoped nanocrystalline silicon film about a micrometer in thickness. Aluminum is then selectively evaporated through a shadow mask in a thermal evaporator at a rate of 15-20Å/s. The base pressure in the evaporator is ~10^{-7} torr prior to evaporation. The contacts thus formed are 5mm in diameter and has a thickness of around 2100Å. The sample is then subjected to successive anneals of 30 minutes duration each at temperatures of

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300°C, 350°C and 400°C in a furnace under nitrogen ambient. The devices were then characterized after each annealing step and the results are shown in the following:

9.2.2 Effects of anneal

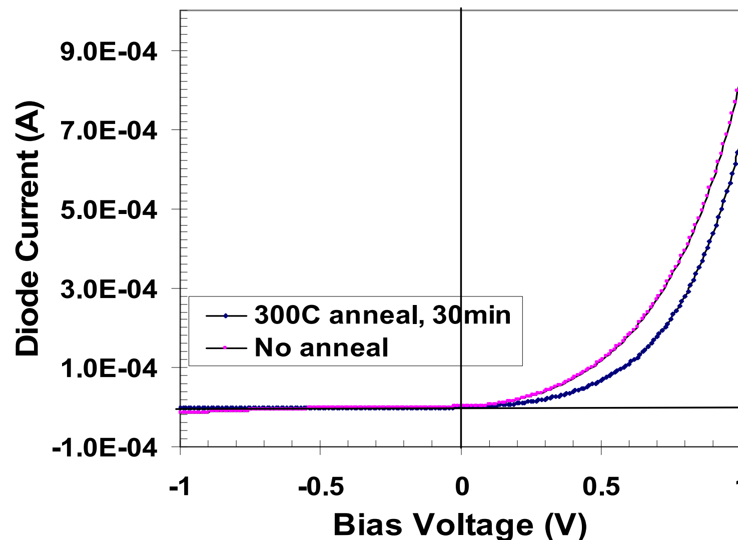

Figure 9.2 Comparison of anneal on diode I-V characteristics

Although at a first glance, the I-V characteristics of the as-deposited and 300°C annealed devices look very similar in figure 9.2, a subtle difference exists. Without any anneal, the Al metal just forms a Schottky contact with the intrinsic nc-Si:H material. We also know from device physics that the I-V characteristics for a Schottky barrier and a p-n junction are similar, except that the ideal reverse saturation current density for a Schottky barrier is orders of magnitude larger than an ideal p-n junction. This is because of the fact that the current in a p-n junction is determined by the diffusion of minority carriers, whereas the current in a Schottky barrier diode is determined by the thermoionic emission of majority carriers over a potential barrier. Due to this difference in reverse saturation current, the Schottky diode turns on at a lower voltage than the p-n junction at

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forward-bias. From figure 9.2 we observe that for the non-annealed device, the turn-on voltage is ~0.3V, while for the 300°C annealed device, the turn-on voltage is ~0.6V, with a lower forward-bias current as expected. This happens because the Al diffuses into the nc-Si:H material upon anneal, and dopes the material p-type, forming a p-n junction as we had speculated.

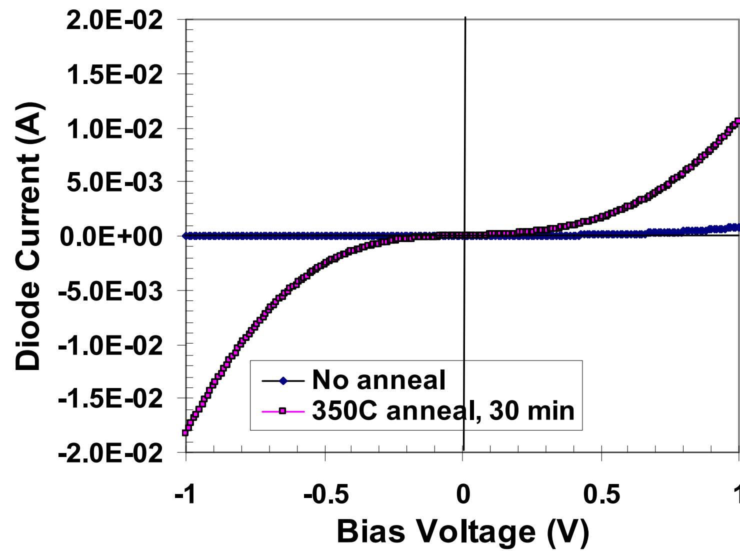

Figure 9.3 Effect of higher annealing on diode I-V characteristics

Comparing figure 9.2 and figure 9.3, we can see that a further annealing of the device for 30 minutes at 350°C, results in a performance loss over the corresponding anneal for 30 minutes at 300°C. The device now shows a significant amount of leakage, and after a 400°C anneal for 30 minutes, the device gets shorted, and no I-V characteristics could be obtained due to current limitations of the Parameter Analyzer. The reason for getting shorts can be many. Primarily, we believe that the Al metal is able to diffuse all through the small thickness of the film at higher anneal temperatures/time and lands up on the n^+ or into the substrate back-contact causing a direct short. Another

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reason can be attributed to the surface roughness of the stainless steel substrate, which can lead to several weak spots/pinholes providing a low-resistance path to the current.

9.2.3 Diode ideality factor

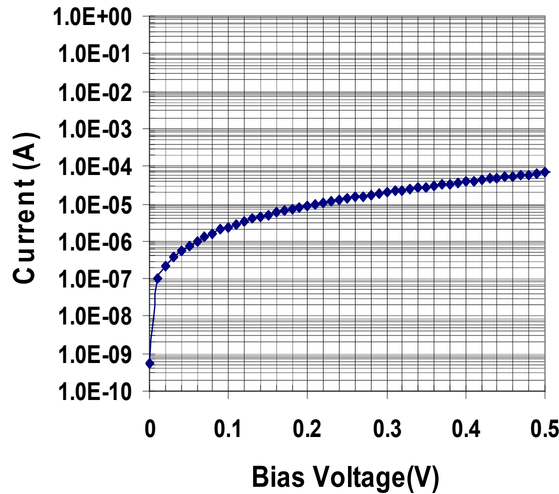

Figure 9.4: Logarthmic plot of forward biased I-V characteristics

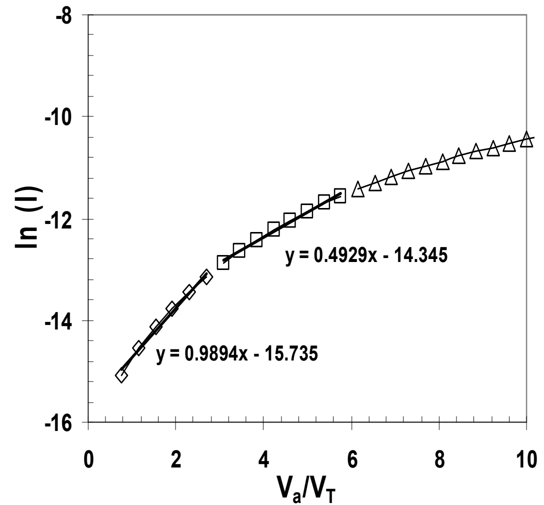

Figure 9.5: Estimation of ideality factor for Al-diffused diode

Figure 9.4 shows the forward I-V characteristics for the diode formed by Al diffusion after anneal at 300°C for 30 minutes on a logarithmic scale. Figure 9.5 shows the recombination and diffusion current components plotted on a log current scale as a function of V_a/V_T.

The total forward-bias current density in a p-n junction is the sum of the recombination and ideal diffusion current densities, and can be written as [**83**].

$$J = J_{rec} + J_D \text{ -- } (1)$$

where J_{rec}, and J_D are given by

$$J_{rec} = J_{r0} \exp\left(\frac{eV_a}{2KT}\right) \text{ -- } (2)$$

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$$J_D = J_S \exp\left(\frac{eV_a}{KT}\right) \text{ -- (3)}$$

and e, Va, K and T are the electronic charge, bias voltage, Boltzmann Constant and temperature respectively.

In general, the diode current-voltage relationship can be written as [83]:

$$I = I_S \left[\exp\left(\frac{eVa}{nKT}\right) - 1\right] \text{ -- (4)}$$

where the parameter n is called the ideality factor. For large forward bias voltage, $n \approx 1$ when diffusion dominates, and for low forward bias voltages, $n \approx 2$ as recombination dominates. From figure 9.5 above, we calculate the values of ideality factors as n_1 = 1.011 and n_2 = 2.029 respectively. These values are very close to the theoretical ideality factors for a p-n junction, and confirms that we have indeed been able to dope the nc-Si:H material p-type by Al diffusion.

9.3 Aluminum Diffused TFTs

9.3.1 Concept and fabrication

In this method of fabricating p-channel nanocrystalline silicon TFTs, we proceed along exactly the same steps as described earlier. The only difference is that we do not deposit the heavily doped p-type nanocrystalline silicon layer and directly proceed to do the metallization instead. After deposition of the nc-Si:H channel, Al was evaporated by thermal evaporation and source and drain contacts were defined by photolithography and etching. The sample was then annealed in a N_2 ambient for one hour at a temperature of 350°C to selectively dope the source and drain regions under the source and drain

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aluminum to heavily p-type. The TFT was then characterized on an HP parameter analyzer.

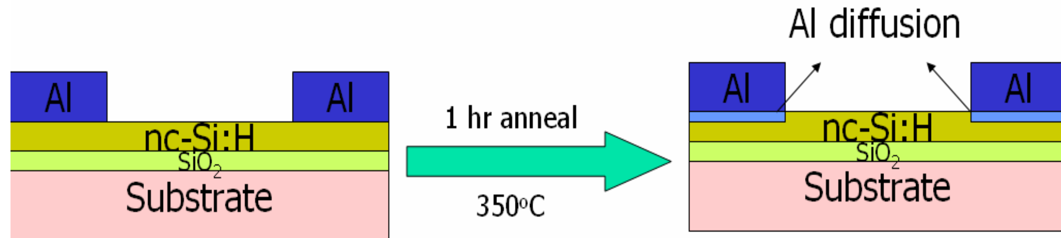

Figure 9.6 Schematic cross section of an Al-diffused bottom gate nc-Si:H TFT

9.3.2 Device characteristics

We report the results for the thin film transistor deposited with an undoped nanocrystalline silicon channel material. For the sake of completeness, devices were fabricated and characterized with varying ppm phosphine doping in the channel, and the results were found to be identical with the devices described in the earlier section. The following figures show the device characteristics for the TFT with aluminum diffused source and drain contacts.

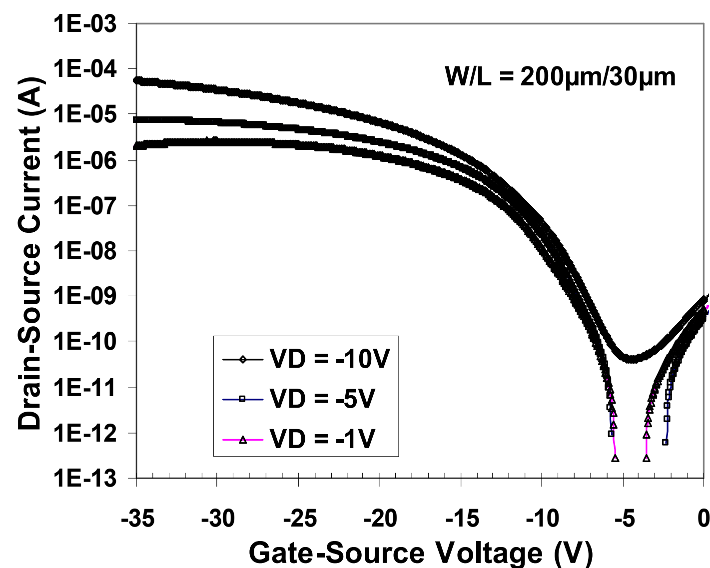

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Figure 9.7 Transfer characteristics of an Al-diffused bottom gate nc-Si:H TFT

Figure 9.7 above shows the variation of drain-source current as a function of gate voltage for the aluminum-diffused TFT at fixed drain-source voltages of -10V, -5V and -1V respectively. The device in this case had a width of 200µm with a drawn channel length of 30µm. The thermally grown gate oxide thickness was 1200Å. The field-effect mobility for this device was calculated to be 1.4cm^2/V-s by a method described earlier, and the threshold voltage is -4.5V. The devices had a high ON/OFF ratio of ~10^7, which is the highest so far in comparable devices of its kind. In these TFTs, the off current is ~10^{-12}A and ~10^{-13}A at drain-source voltages of -5V and -1V respectively. Such low OFF current values is a representative of low defect and impurity levels in the nc-Si:H channel material, and that we are not adding any more impurities into the channel under Al diffusion.

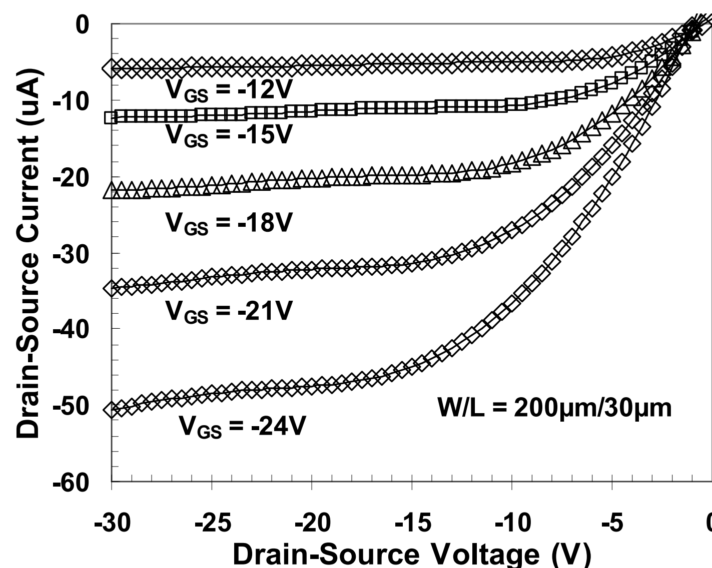

Figure 9.8 Output characteristics of an Al-diffused TFT at varying gate voltages

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Figure 9.8 shows the output characteristics of the bottom gate nc-Si:H p-channel TFT formed by selective Al diffusion for the source and drain regions. The output characteristics resemble classical p-channel MOSFET characteristics with no evidence of any current crowding at low-drain to source voltages. Therefore, we have been able to show that low-temperature Al diffusion can be employed to dope nc-Si:H heavily p-type and form low series resistance contacts for the source and drain regions of p-channel TFTs.

9.3.3 Discussion

In this work, we have systematically demonstrated for the first time a very simple method of doping nanocrystalline silicon p-type using low temperature aluminum diffusion. Firstly, by forming a n+/n/Al structure and then performing a low temperature Al diffusion we have shown how the output I-V characteristics changed from a Schottky barrier to that of a classical p-n junction upon anneal. Secondly, we have extended this concept to selectively dope the source and drain regions by Al diffusion to obtain classical p-channel MOSFET behavior from nc-Si:H TFTs. The greatest advantage of this process is that the fabrication becomes a lot simpler eliminating extra photolithography and dry-etching steps. A logical extension of this process would be to fabricate CMOS type thin film devices, where a selective doping using Al diffusion would lead to a huge process simplicity/cost advantage.

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CHAPTER 10. ADVANCED DEVICE CHARACTERIZATION

10.1 Introduction

In the previous section, we were mostly interested in an overall characterization of thin film transistor devices and basic parameters like mobility, threshold voltage, and subthreshold slope were obtained by plotting drain current against gate voltage. There are some other fundamental parameters which can be extracted by a more rigorous characterization, and can provide us with useful insights into the physics involved. In this chapter, we would describe some of these characterization techniques used in obtaining the series resistance of contacts, the resistance of the channel material, and also the maximum defect densities at the interface and bulk. We would also report on the mobility and threshold voltage values obtained by an independent measurement, and compare the results and limitations, if any.

10.2 Transmission Line Method

10.2.1 Theory of TLM

In the linear regime of operation i.e. at low drain voltage, and using the gradual channel approximation for MOSFETs [83] we have

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} (V_G - V_T) V_{DS} \text{ ------------------------------- (1)}$$

Here, μ_{FE} is the field effect mobility, C_{ox} the oxide capacitance, W is the width and L is the length of the MOSFET. V_G, V_T and V_{DS} are the gate voltage, threshold voltage and drain-source voltages respectively.

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The above equation predicts that for low drain-source voltages, we can observe a linear characteristic between the drain current and gate voltage. For a complete analysis of the electrical performance of the thin film transistor, we need to extract the TFT source and drain series resistances, the intrinsic threshold voltage and the intrinsic field effect mobility. The intrinsic device parameters are a measure of the electrical characteristics of the conduction channel itself without the influence of parasitic series resistances [86]. These are extracted by the well known Transmission Line Method [87] by using a series of TFTs having different channel lengths and measured under low source to drain voltage so that any space charge limited current (SCLC) effects can be neglected.

The total ON resistance for the TFT under consideration is given by

$$R_T = \frac{V_{DS}}{I_D} = r_{ch}L + R_S + R_D \text{ ------------------------------ } (2)$$

where r_{ch} is the channel resistance per unit length and R_S and R_D are the source and drain series resistances respectively [86]. Using equations 1 and 2 we can express the total ON resistance of the TFT and a function of the threshold voltage and apparent field effect mobility as

$$R_T = \frac{L}{\mu_{FE} C_{ox} W (V_G - V_T)} \text{ ---------------------------------- } (3)$$

Considering the ideal case of negligible contribution to series resistance from the source and drain, we can express the channel resistance as a function of the intrinsic field effect mobility (μ_i) and threshold voltage (V_{Ti}) as

$$r_{ch} = \frac{1}{\mu_i C_{ox} W (V_G - V_T)} \text{ ----------------------------------- } (4)$$

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10.2.2 Experimental results

The extraction of the TFT source and drain series resistances and intrinsic threshold voltage and field effect mobility is now easy to calculate using a series of TFTs with varying channel lengths. For calculating these, we first calculate the ON resistances as a function of TFT channel length at varying gate voltages. Care must be taken so that the voltages are low enough to keep the TFTs in accumulation region of operation. The experimental data is then fitted to obtain linear plots as shown in fig 10.1 below.

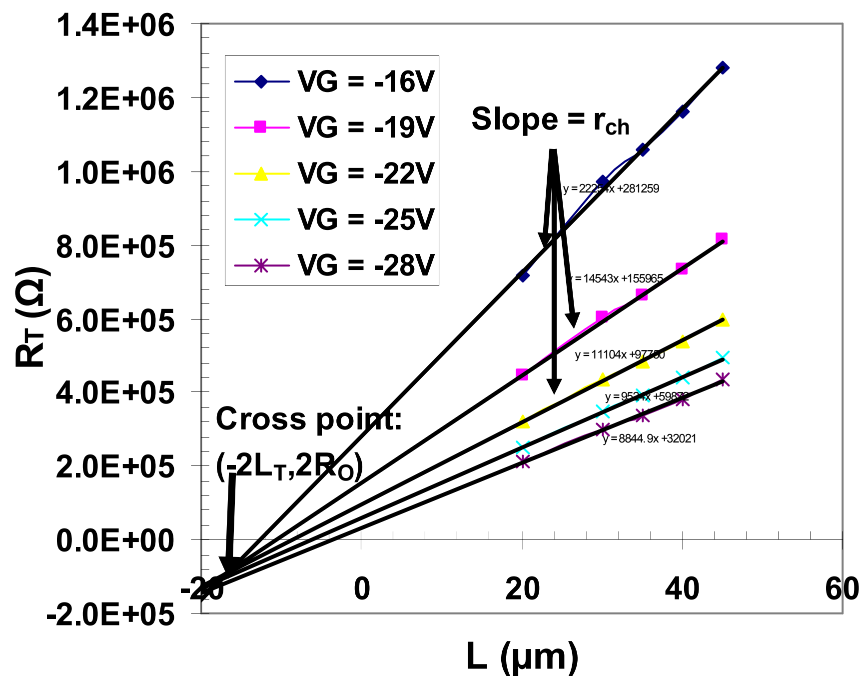

Figure 10.1 Illustration of the TLM used to extract the TFT source/drain series resistances

From the above linear fits to the experimentally observed data, we can obtain the total TFT series resistances ($R_S + R_D$) from the y intercepts and the channel resistance per channel length (r_{ch}) from the slopes.

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We then proceed by plotting the reciprocal of r_{ch} as a function of the gate voltage and perform a linear fit. The slope then indicates the intrinsic field effect mobility (μ_i) as evident from equation (4) and we obtain the intrinsic threshold voltage (V_{Ti}) from the x-intercept as shown in figure 10.2 below.

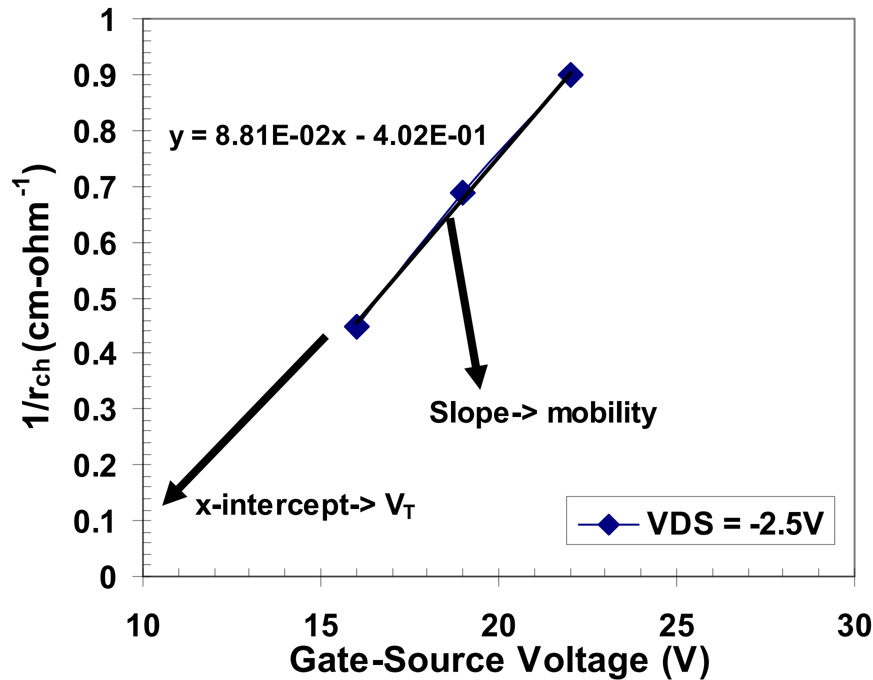

Figure 10.2 Extraction of the TFT intrinsic parameters using TLM

From the above figure, we estimate the values of mobility and threshold voltage from the slope and intercept respectively to be:

μ_i = 1.607 cm^2/V-s $\qquad$ V_{Ti} = -4.56 V

These values compare well with our experimentally observed values of mobility and threshold voltage at μ_{FE} = 1.60 cm^2/V-s, and V_T = -4.5 V in the case of independent measurement of drain-source current versus gate-source voltage.

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10.2.3 TFT characteristic length

Due to the effect of series resistances, the current is a bit smaller and can be modulated as an apparent increase in the channel length. The total TFT ON resistance can be written as [86]:

$$R_T = \frac{V_{DS}}{I_D} = R_S + R_D + \frac{L}{\mu_i C_{ox} W(V_G - V_T)} \text{ ----------------------- } (5)$$

$$R_T = 2R_O + \frac{L + 2\Delta L}{\mu_i C_{ox} W(V_G - V_{Ti})} \text{ ---------------------------------- } (6)$$

where R_O represents the limit of the source and drain series resistances for a very high gate voltage and can be associated with the contact resistance of source and drain. ΔL is independent of the gate voltage and can be associated with the resistance of the access region between the conduction channel and the source and drain contacts [87].

As shown in figure 10.1, ΔL and R_0 can be extracted from the R_T versus L curves. All of the R_T versus L curves have a common cross point located slightly away from the y-axis [87], the coordinates of which are given by ($x = -2\Delta L$, $y = 2R_0$). We thus have:

$$\Delta L = 8\mu m,\ R_0 = R_S + R_D = 50K\Omega$$

The series resistances for a TFT bear a strong correlation to the overlap between the source/drain contact and the gate contact. It has already been shown that the TFT contact resistance is not governed by the entire overlap between the gate and drain and is limited to a specific area of the contact [90-92]. We can thus define a TFT characteristic length (L_T) to represent contact area [86] as shown in the figure below.

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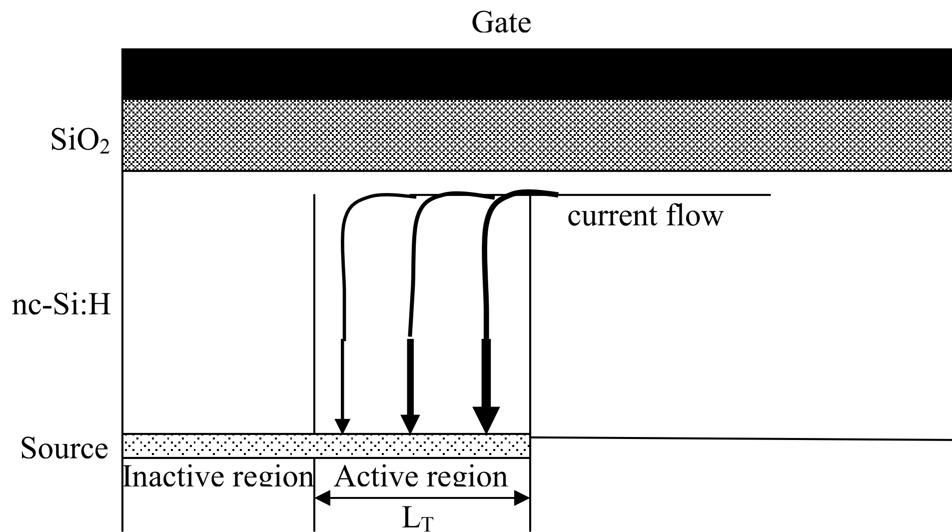

Figure 10.3 Definition of the characteristic length L_T at the source and drain contacts [86]

This characteristic length increases with the nanocrystalline silicon thickness, the bulk defect density and the source and drain contact resistances [93]. The effective source/drain series resistivity (r_{Ceff}), defined as the sum of the drain/source resistivity and the resistivity associated with the bulk of the access region between the contact and conduction channel [92] is given by

$$r_{Ceff} = W\, L_T^2\, r_{ch} \quad (7)$$

using equation 7, and W =200µm, L_T = 8µm, r_{ch} = 11.1 KΩ/µm

$$r_{Ceff} = 1.42\Omega\text{-cm}^2$$

The source/drain contact characteristic length (L_T) is very important from a TFT designing point of view for optimal device performance. During mask design, we would like to keep the overlap region between the source/drain at least equal to or greater than the characteristic length. This is because for an overlap smaller than L_T, the whole contact is active. As the contact resistance is inversely proportional to the area, we have a larger contact resistance by keeping the overlap too small.

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10.2.4 Discussion

In our device design, the overlap between the source/drain and gate was kept at 15μm. From the above analysis, we find that the contact characteristic length for our device for a given set of deposition parameters was 10μm. In this way, we are safely out of the domain where our device performance could be limited by contact resistance problems. As a note, we should mention that our simplified bottom gate TFTs had a full overlap between the source/drain and gate contacts. The penalty we pay for any increase in the overlap area is an increase in the TFT parasitic capacitance. For this work we were not much interested in switching speed of devices, and could ignore this. A scope of improvement lies in reducing this overlap in the next mask design to optimize device performance.

10.3 Transconductance method

Another method of estimating the mobility of a MOSFET device is by the well known method of transconductance measurement. For a TFT operating in the linear region, the field-effect mobility is given by [85]:

$$\mu_{FE} = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)\frac{L}{C_{ox}V_{DS}W} \text{ -- (8)}$$

Here, $\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)$ is the transconductance of the device obtained directly from the HP Parameter Analyzer and C_{ox} is the silicon dioxide gate capacitance per unit area. The following figure 10.4 illustrates the experimentally observed mobility as obtained using equation (8).

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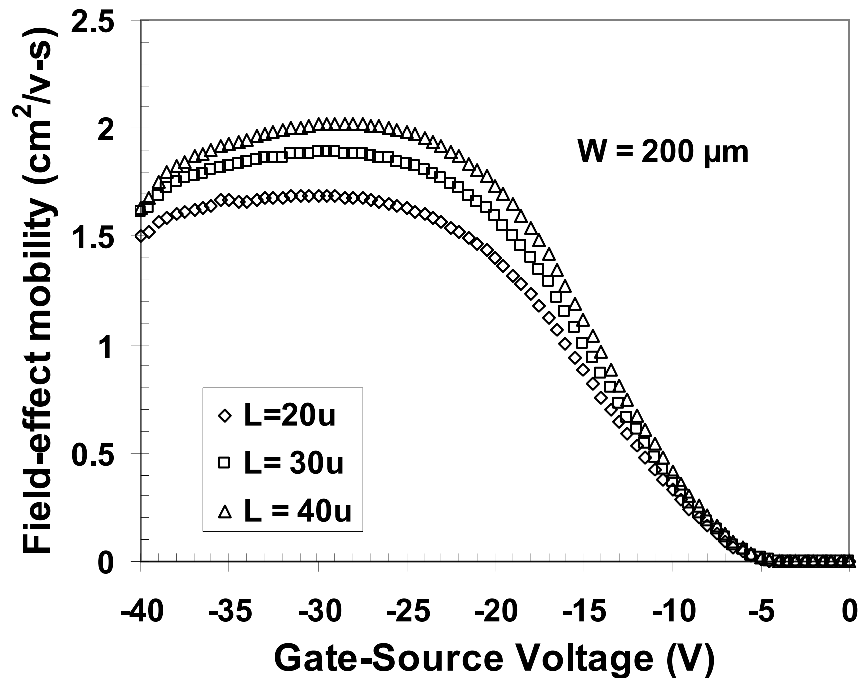

Figure 10.4 Transfer characteristics of a TFT from transconductance measurements

From the above plot, we can observe two regimes of mobility behavior for the TFT under consideration. At low gate to source voltages, the mobility is controlled by the band tail state density in nanocrystalline silicon channel material. At higher gate-source voltages, the mobility is limited due to scattering effect of holes. Also, the apparent decrease in mobility with length of the channel signifies that the series resistances from the contacts start playing an increasing role relative to the resistance of the channel.

10.4 Maximum defect density characterization

10.4.1 Theory

As discussed in the previous section, diffusion dominated current transport comes into play once the drain voltage (V_{DS}) is larger that a few KT/q, and the subthreshold

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current becomes independent of the drain voltage. On the other hand, the dependence on the gate voltage is exponential with a subthreshold slope given by [25]:

$$S = 1/\left(\frac{d(\log_{10} I_{DS})}{dV_g}\right) = 2.3\,\frac{mKT}{q} = 2.3\,\frac{KT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right) \text{---------------} (9)$$

Here $m = \left(1+\frac{C_{dm}}{C_{ox}}\right)$ gives us a measure of the interface trap density since the capacitance associated with the interface trap is in parallel with the depletion layer capacitance (C_{dm}).

In particular, the subthreshold slope depends on the trap density in the bulk (N_T) and at the interface between nanocrystalline silicon and silicon dioxide gate dielectric [85]. The subthreshold slope can then be approximated as [94]:

$$S = qK_BT(N_Tt_s + D_{it})/C_{ox}\log_{10}e \text{ --------------------------- } (10)$$

Here q, K_B, T, t_s and C_i are respectively the electronic charge, the Boltzmann constant, the absolute temperature, the nc-Si channel layer thickness, and the silicon dioxide gate dielectric capacitances. From equation (10), we can estimate the maximum values of N_T and D_{it} by separately setting each of them to zero.

10.4.2 Experimental results

Let us consider the case for the device where the nanocrystalline silicon channel was undoped, giving us a minimum subthreshold slope of 700mV/decade. The gate-oxide thickness is 1200Å, and the thickness of the nc-Si:H channel layer (t_s) is 100nm. Now setting N_T and D_{it} to zero separately, we have the estimate of maximum defect densities as:

$D_{itM} = 2.10 \times 10^{12}\ cm^{-2}eV^{-1}$ $N_{TM} = 2.1 \times 10^{17}\ cm^{-3}eV^{-1}$

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10.4.3 Discussion

The maximum value of N_T is reasonable, considering the inhomogeneous nature of the nanocrystalline silicon material, with numerous grain boundaries and defect states. Moreover, the channel formed in this case is interface layer between oxide and nanocrystalline silicon, where growth just starts. We believe that the defect density can be reduced even further by using a top-gate device geometry, where the channel is formed at the more homogenous nanocrystalline silicon bulk interface. However, the maximum value of oxide interface defect density is large compared to best values of $\sim 10^{11} cm^{-2} ev^{-1}$ for MOSFET devices. This can be due to the fact that some amount of plasma damage happens during the growth of the nanocrystalline silicon phase, or due to the fact that the higher defect density in the nc-Si:H material is masking the oxide defect in equation (10). Again, a top-gate device is expected to give smaller density of defects at the oxide interface, since the oxide deposition conditions are much mild as compared to nanocrystalline silicon, where high plasma power growth is usually required. As a passing note, it may be mentioned here that the maximum values of defect densities are lower than or comparable to similar values reported in literature [84].

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CHAPTER 11. TFT STABILITY

11.1 Introduction

For reliable operation, it is important that the TFTs exhibit a high stability under prolonged gate bias stress. An ideal TFT should show little or negligible shift in threshold voltage without any appreciable change in mobility after being subjected to stress. Generally two mechanisms are responsible for the observed degradation in TFTs: charge trapping in the gate insulator and defect state creation in nc-Si:H. In chapter we would briefly discuss the main defect creation mechanisms, and compare our experimentally observed results obtained by stressing TFTs.

11.2 Mechanism of charge trapping in SiO_2

The well observed phenomena of charge trapping in silicon dioxide can be attributed to processes originating from its bonding structure. Wang [95] proposed the bonding arrangements of silicon atoms in silicon dioxide films and also on the surface of crystalline silicon wafers. A silicon atom should necessarily have four nearest neighbors to satisfy the covalent bond requirements, while a surface silicon atom would be required to have only three neighbors. An electron with unpaired spin would therefore be associated with this surface silicon atom, forming a dangling bond. This dangling bond acts as an electron trap, since it is ready to accept an electron to complete the covalent bond.

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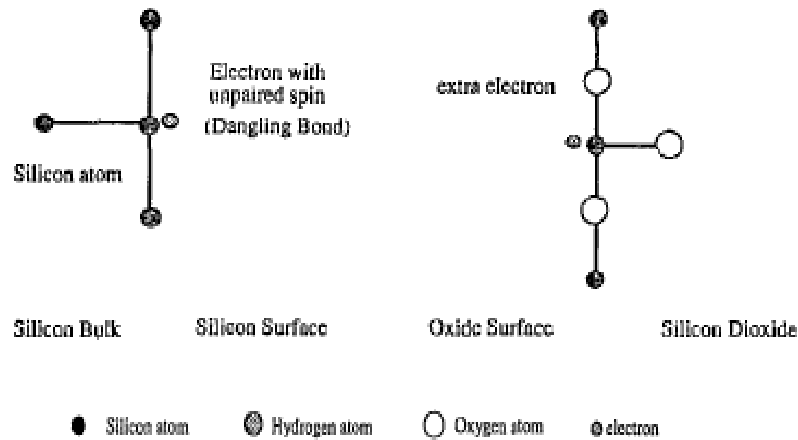

Figure 11.1 Schematic diagrams of silicon atom at silicon surface and silicon atom at the oxide surface with their trapping effect [47]

The bonding requirements for SiO_2 are quite in discrepancy from those of Si, as it is easy for electrons to transfer from silicon to oxygen [47]. However, a silicon atom over an oxide film has only three neighboring oxygen atoms. In this way, the silicon atom is incapable of transferring its extra electron, and is shown in the figure above. A silicon atom on silicon surface (Si_{ss}) requires an electron for completion of its covalent bond, while a silicon atom on oxide surface (Si_{os}) has an extra electron. This extra electron is mutually transported in a natural process completing the Si-SiO_2 bond, as shown below.

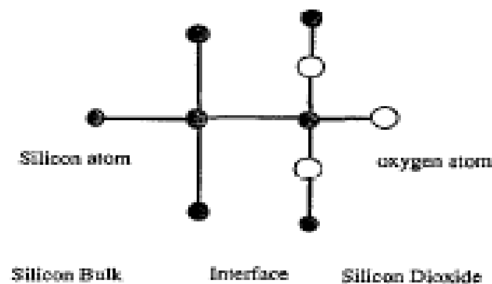

Figure 11.2 Schematic showing Si and SiO2 satisfying the covalent-bond requirement [47]

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A model of trap generation due to oxygen vacancies was forwarded by Woods and Willians [96], in which an oxygen atom was first removed from the tetrahedral structure, and two silicon atoms formed a Si-Si bond across the vacancy. These silicon atoms remained approximately in their original position, with the center forming a neutral hole trap and becoming positively charged by losing the non-bonding electron. This is schematically represented in figure 11.3.

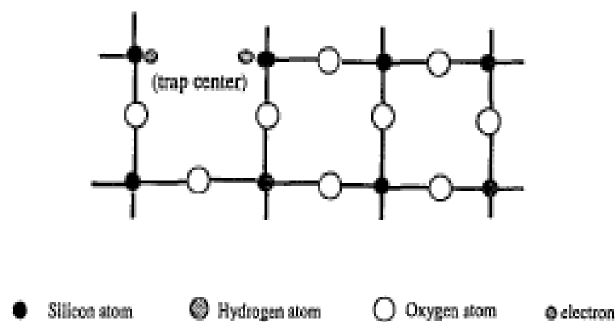

Figure 11.3 Illustration of oxygen vacancy in the oxide [47]

Another trapping mechanism at the interface has been proposed by Jeppson and Svensson to explain the degradation of MOS devices under negative-bias stress [97]. A two dimensional model similar to the previous one was proposed, in which an oxygen vacancy is incorporated with the trapping center in the bulk of the oxide. This trapping center is compensated for by capturing an electron from hydrogen atom following a post-metallization-anneal treatment, and is illustrated in figure 11.4. This H atom has originated in the SiO_2 bulk or the Al-SiO_2 interface.

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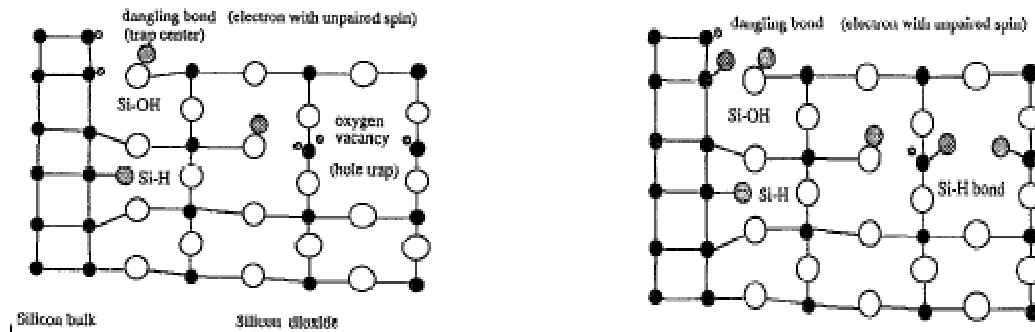

Figure 11.4 PECVD SiO_2 films (a) prior to post metallization annealing, (b) following post metallization annealing [47]

However, after a bias-temperature or current-voltage stress, the surface defect Si_{ss}-H which had become inactive after PMA becomes electrically active. The hydrogen atom weakly bonded to the surface silicon can react with Si-O in the bulk of SiO_2 forming a silanol Si-OH bond. In this process, one Si^+ in the oxide and one trivalent surface trap Si_{ss} would be left forming many unbonded trapping centers, as shown in figure 11.5.

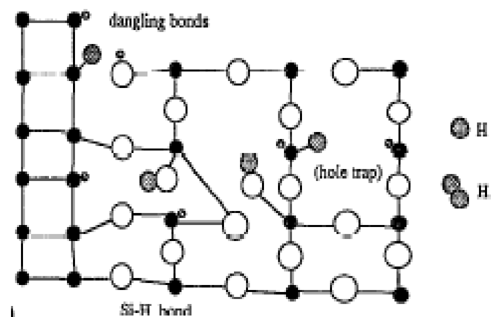

Figure 11.5 PECVD SiO_2 films following current, voltage, or bias temperature stress [47]

11.3 Mechanism of charge trapping in nanocrystalline silicon

It is now well known that nanocrystalline silicon consists of columnar grains with some amorphous tissue. PECVD nc-Si:H silicon growth starts off initially from an

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amorphous phase and the grain boundaries become well defined after the film has grown to a certain thickness. This means that the diameter of the columns are not uniform along the growth direction, being tapered initially and gradually increases with growth attaining saturation. Moreover, there are many defect states along the grain boundaries with the bottom phase contributing the most on account of its larger amorphous content and porosity. It may be mentioned that by controlling the growth conditions, many of these defects can be passivated by hydrogen, but more work still remains to bring this down to levels comparable to single crystal silicon. The following figure shows a rough schematic of a typical nanocrystalline silicon film with the amorphous phase and defect states.

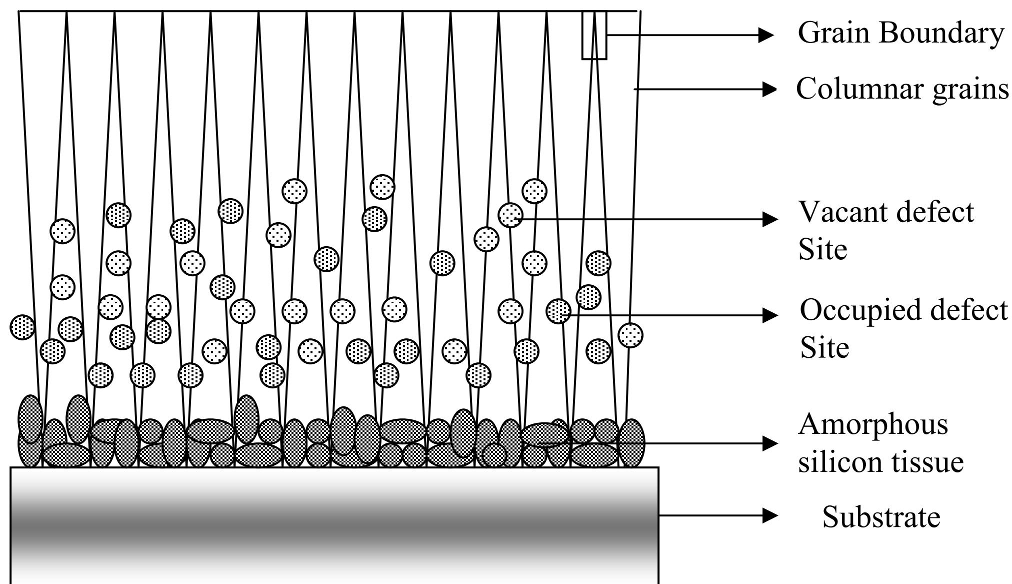

Figure 11.6 Structure of a typical nc-Si:H film with trapping centers [6]

As can be seen from the above, these defects can either be in the acceptor or donor state and are able to capture or donate an electron. A qualitative description of the physical phenomenon in n-channel nc-Si TFTs was proposed [105], and in this work we would explain our results in the context of p-channel nc-Si TFTs.

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11.4 Device characteristics from stressing experiments

To test the stability of the nanocrystalline silicon channel material, stress experiments were performed by applying negative and positive gate bias of -30V and +30V respectively. This corresponds to a high electric field of about 2.5MV/cm across the thickness of the oxide. The source was grounded, while a voltage of -5V was applied to the drain terminal. The devices were subjected to a stress time totaling 10^5 seconds, and data was recorded promptly at different time intervals taking care so as not to disturb the stressing conditions. In order to avoid any stress-induced history effects, positive and negative stress were performed on separate, but identical devices. The stressed devices were allowed to relax for 3-4 hours in ambient, and the output characteristics were recorded. From the drain current against gate voltage output characteristics, field effect mobility and threshold voltages were calculated and the results are shown in the following:

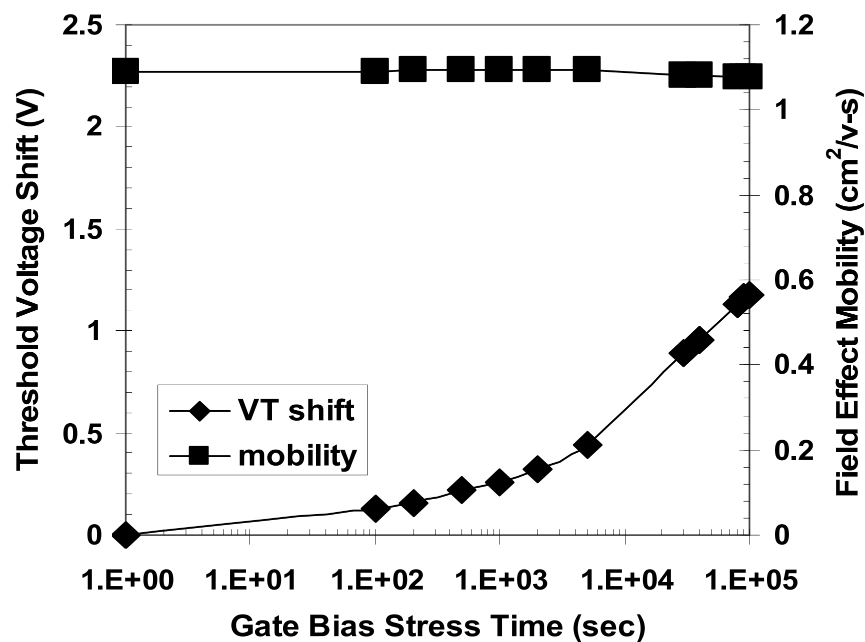

Figure 11.7 Shift in threshold voltage and mobility under negative gate bias stress as a function of time

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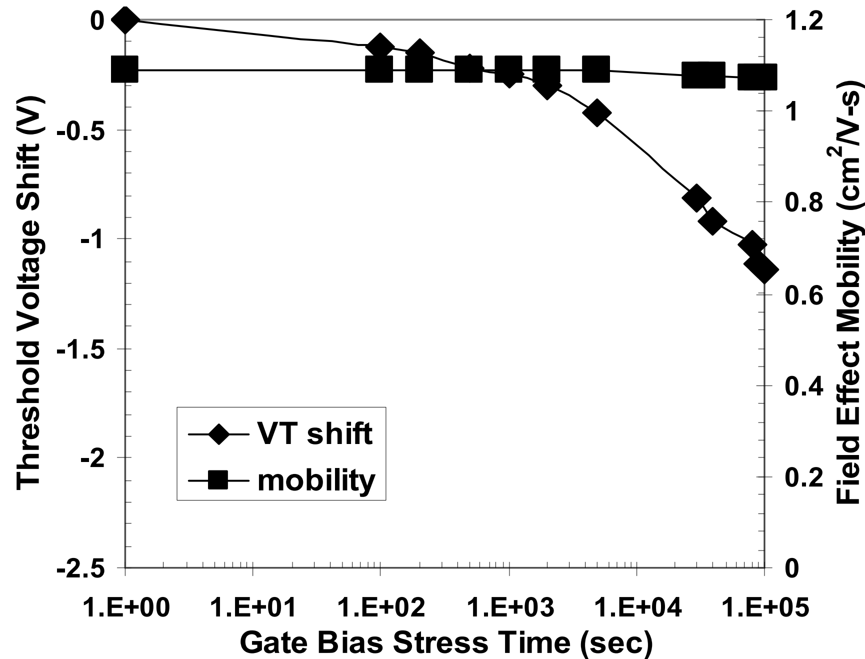

Figure 11.8 Shift in threshold voltage and mobility under positive gate bias stress as a function of time

From the above plots, we find that the change in mobility after prolonged gate bias stress is negligible. We cannot conclude anything with the small mobility degradation observed as it would fall within the limits of experimental error. The threshold voltage increases under a negative gate bias stress and decreases under a corresponding positive gate bias stress. The majority of the threshold voltage shift occurs during the initial stages of stressing in both cases.

In this context, it is worthwhile to note that the TFTs subjected to either positive or negative gate bias stress recovered to the as-deposited state after 4-5 hours in ambient. We thus suspect that the shift in threshold voltage is a result of temporary charge trapping

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in the nc-Si:H channel material as a result of gate bias stress, and not due to the degradation of the material itself.

The following figure shows the drain current versus source-drain voltage characteristics for a device measured before stress and after negative and positive gate bias stress respectively for 10^5seconds. For each of these measurements, the gate voltage was fixed at two different values of -15V and -20V.

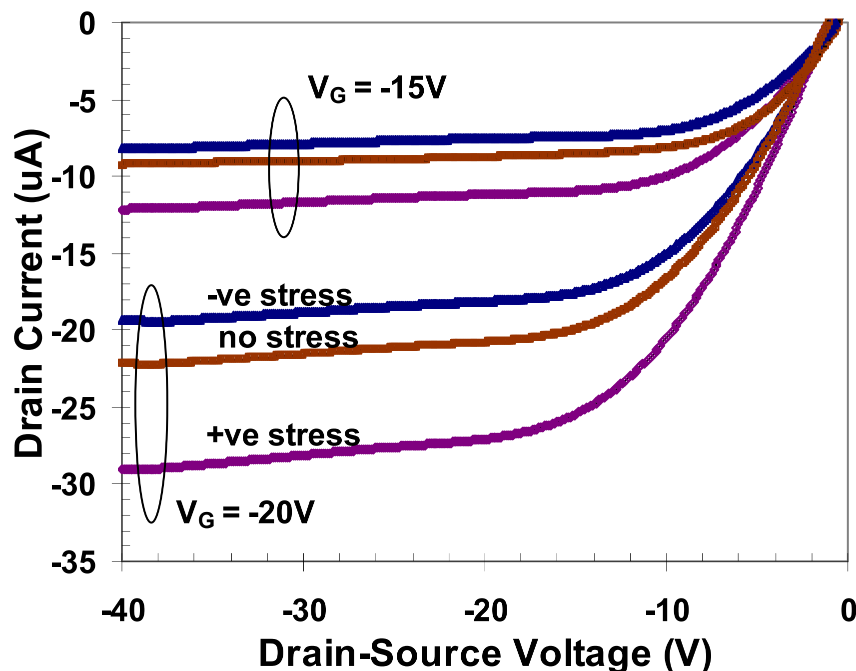

Figure 11.9 Comparison of drain saturation currents under no stress, and positive and negative gate bias stress

From the above figure, we find that the drain saturation current decreases for the device subjected to a negative stress as compared to the as-deposited device. The drain saturation current on the other hand increases when the device is subjected to a positive gate bias stress. Comparing these results to those in figures 11.7 and 11.8 provides us with an intuitive idea about the overall phenomena. The threshold voltage becomes more

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negative/increases under negative gate bias stress, while the same becomes less negative/decreases under positive gate bias stress. The overall drive current is proportional to the gate voltage modulated by the threshold voltage, and so the saturation current increases when the threshold voltage decreases and vice versa.

11.5 Discussion

As all the results of this study indicate, the increase in threshold voltage after negative gate bias stress and the decrease in threshold voltage after positive gate bias stress is a result of temporary charge trapping in the gate oxide or at the nanocrystalline silicon channel material/ oxide interface. The gate dielectric used in this study was thermally grown silicon dioxide and is of a very high quality. For this reason, charge injection into the bulk of the oxide can be safely neglected. There have been some reports that silicon films deposited by CVD form a better interface with silicon nitride as compared to oxide [98-100]. Also, many of the interface traps can be attributed to the nature of the nanocrystalline silicon material formed during growth. In the initial stages of growth, the film has more amorphous content and a greater porosity, and it is this region where the interface with gate-oxide is being formed. By using a very hydrogen dilution and reducing the growth rate at this initial phase, we were able to obtain a high quality interface, the indicative of which is the small and temporary threshold voltage shift during stress accompanied by negligible or no reduction in the mobility.

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CHAPTER 12. CONCLUSIONS AND FUTURE RESEARCH

In conclusion, in this thesis, in contrast to all previous work, we have shown that it is possible to fabricate true n-body, p channel bottom gate thin film transistor devices in nanocrystalline Si:H films. We showed that by doping the body layers with ppm levels of phosphine during deposition, it was possible to increase the body doping and simultaneously, increase the threshold voltage, as expected from standard MOSFET theory. The threshold voltage was shown to increase approximately as square root of phosphine flow, as expected from theory.

We also show that very high on/off current ratios, exceeding $1x10^7$ can be obtained in these devices. The ratio initially increases as the phosphine doping increases, as expected. However, at higher doping levels, the surface leakage reduces the ratio. We also show that a top-layer of PECVD deposited oxide reduces the leakage current.

The mobility values achieved in our TFT devices are among the highest reported in the literature and exceed 1 cm^2/V-s.

We show that a simple Al diffusion process can be used to fabricate the device. This simple process obviates the need for making separate drain and source regions by PECVD growth and subsequent RIE etching to separate the source and drain regions. In our process, a deposition of Al, followed by wet etching to define the source and drain regions, and subsequent diffusion, makes good source and drain p type contacts. No post-deposition reactive ion etching is needed. Avoiding such RIE prevents surface damage and excessive leakage, thus allowing us to obtain high on/off ratios.

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We show that by using helium instead of hydrogen as the diluent gas for the growth of nanocrystalline silicon p layers, followed by subsequent annealing, results in significant increase in the conductivity of such p layers. We ascribe this increase to helium preventing 3-center bonding of boron to silicon.

Further research should focus on understanding of the cause of high threshold voltages, and on the fabrication of top-gate TFT devices which can be expected to have higher mobilities.

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